

# LNSTRIP read-out ASIC for the X-ray strip detectors

Weronika Zubrzycka-Singh

**Abstract**—The X-ray imaging systems dedicated for X-ray spectroscopy, based on a semiconductor strip sensors have been recently an important research topic. The most important research objective is working towards improvement of the spectroscopic and position resolution features [1]–[3]. In spectroscopic applications the short strip silicon detectors are widely used due to their relatively small capacitance and leakage current. Using strip pitch below  $75\ \mu\text{m}$  enables achievement of high spatial resolution. In this work, the analysis and design of the read-out electronics for the short silicon strip detectors are presented. The Charge Sensitive Amplifier (CSA) is optimized for the detector capacitance of about  $1.5\ \text{pF}$ , and the shaping amplifier default peaking time is about  $1\ \mu\text{s}$  (controlled by the sets of switches). To achieve the lowest possible noise level, the sources of noise in a radiation imaging system both internal (related to the front-end electronics itself), as well as external, were considered [4]. We target the noise level below  $40\ \text{el. rms}$ , considering low power consumption (a few mW) and limited channel area. To increase the speed of incoming hits processing, the continuous-time resistive CSA feedback together with a digital feedback reset are included. The prototype integrated circuit comprises of 8 charge processing channels, biasing circuits, reset and base-line restoration logic, and a calibration circuit.

**Keywords**—front-end electronics for detector readout; Si microstrip detectors; X-ray detectors; VLSI circuits

## I. INTRODUCTION

THE requirements for the X-ray imaging techniques and devices for spectroscopy applications include high energy resolution, high dynamic range and count rate (for counting purposes) and the good spatial resolution. Achieving high X-ray spectroscopy resolution is possible only if the front-end electronics meets the requirement of low equivalent noise charge (ENC), but at the same time the read-out electronics should enable handling high input count rates. In the multi-channel systems for spectroscopic applications, it is also very important to obtain good parameters uniformity (between all read-out channels) so that it is possible to distinguish between spectral lines of radiation. This paper presents the design and optimization of the prototype read-out ASIC dedicated for 1D silicon strip detectors with  $75\ \mu\text{m}$  pitch. For the noise optimization it was assumed that each of the sensor electrodes is  $1\ \text{cm}$  long and exhibits a capacitance of around  $1.5\ \text{pF}$ . In this project the aim was to minimize the total noise by proper optimization of the charge processing chain, to achieve ENC

lower than  $40\ \text{el. rms}$ , without compromising the maximum input count rate processed by the front-end [5]–[7]. To make it possible, some digital supporting circuits were implemented (fast reset of the CSA and base-line restoration). The targeted energy range is  $4\text{--}10\ \text{keV}$ , and the nominal signal of  $2200\ \text{el.}$ , which corresponds to the charge generated by  $8\ \text{keV}$  in a silicon detector.

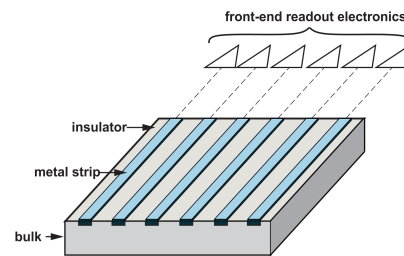


Fig. 1. Single-sided strip detector.

## II. THE CIRCUIT OVERVIEW

The prototype front-end ASIC presented in Fig. 2 consists of 8 read-out channels. Each of the channels contains full charge processing chain comprising of a charge sensitive amplifier (CSA), a shaping amplifier and a discriminator. Additionally, digital control circuits for the fast CSA reset and base-line restoration are included.

The CSA core is based on the telescopic cascode architecture with a PMOS transistor as the input device with the aspect ratio selected to match its capacitance to the detector capacitance ( $W/L = 240/0.2\ \mu\text{m}$ ). The core amplifier gain is equal to  $6.1\ \text{kV/V}$ , the GBW  $1\ \text{GHz}$  and the dissipated power does not exceed  $4\ \text{mW}$  (assuming CSA input transistor bias current of  $1\ \text{mA}$ ). The CSA feedback capacitor value is  $50\ \text{fF}$  which results in a  $20\ \text{mV/fC}$  gain. The feedback resistor is realized using a MOS transistor working in the linear region and the nominal value is  $10\ \text{G}\Omega$ .

The identification of all of the noise components was conducted to minimize their contributions and to make sure that the total noise of the charge processing chain is dominated by the CSA input transistor thermal and flicker noise. The main noise components of the CSA core are (see Fig. 3):

- input transistor (M1) thermal noise - taking into account the dependence of the thermal noise on the bias current, the regulation of this parameter is provided,

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Front-end overview

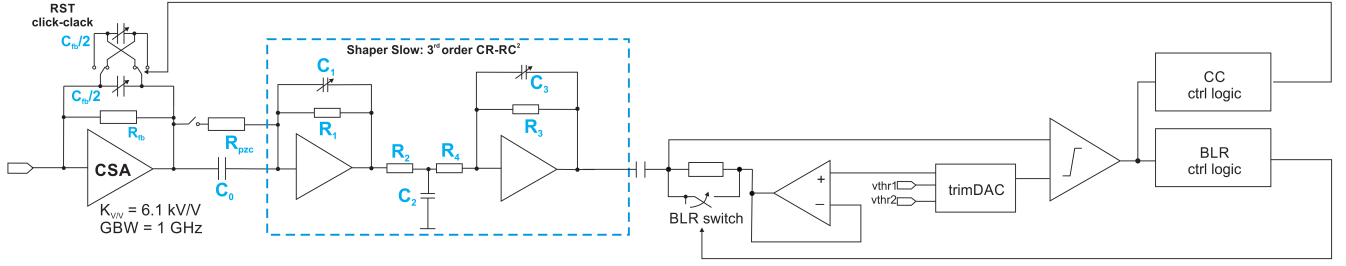


Fig. 2. Charge processing chain schematic.

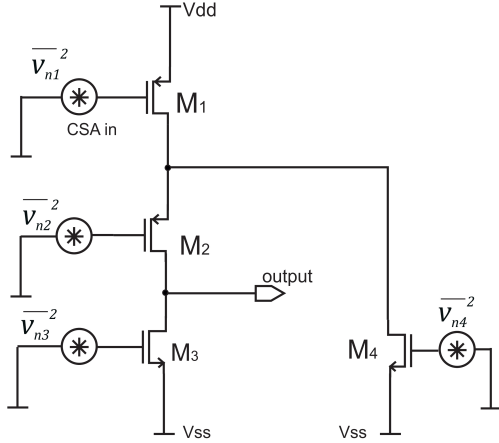


Fig. 3. Noise sources in the CSA core based on a telescopic cascode architecture.

- amplifier bias current source (transistor M4) - decrease the transconductance,
- amplifier load transistor thermal noise (transistor M3) - decrease the transconductance.

The noise introduced by the remaining transistors was reduced by modification of their sizes [8].

In order to minimize the impact of current sources on noise performance, it is necessary not only to lower their thermal and white noise spectral densities, as well as their transconductance values. Special attention should also be given to noise arising from the biasing of these sources (see Fig. 4). One effective method to reduce noise introduced by the global current source and associated coupling effects is to scale down the global reference current by a factor B within the channel.

While several components in the system contribute to ENC, the primary focus of this analysis is on the sensor. Key factors affecting noise from the detector side include leakage current and strip capacitance. As shown in Figure 5, total output noise increases with detector capacitance, and even small sensor leakage currents (40–50 pA) significantly raise the constant term in the noise equation 1, as illustrated in Figure 6. Since leakage roughly doubles every 8°C, effective cooling is essential [9].

$$ENC = 8e^- + C_{det} \cdot 5.6e^- / pF \quad (1)$$

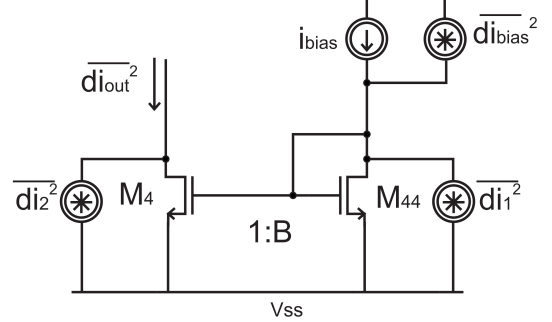
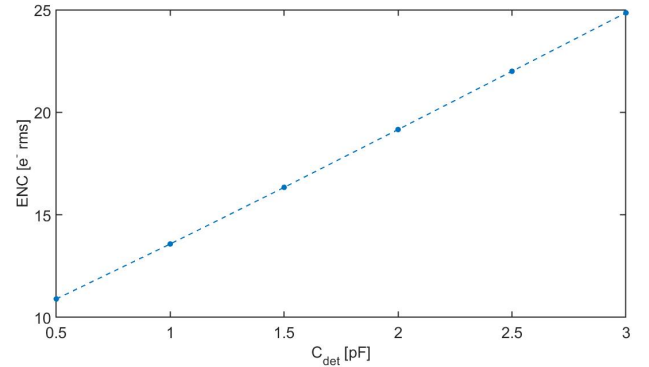


Fig. 4. Noise in the biasing current mirror.

Fig. 5. ENC vs. detector capacitance (no leakage current,  $R_f$  not noisy).

Although external parasitic elements also impact noise performance [4], these are minimized through careful detector selection and optimized PCB and interconnect design.

The design and parameters of the shaping amplifier were selected basing on the noise optimization of the front-end. The type, order, and shaping time of the filter play a crucial role in determining the overall output noise of the charge processing chain. In this project, several shaping amplifier configurations were analyzed through simulation, including semi-Gaussian  $CR-RC^n$  structures and higher-order filters featuring complex conjugate poles of 3<sup>rd</sup> and 5<sup>th</sup> order. Based on the obtained Equivalent Noise Charge (ENC) values and considering power constraints, a straightforward  $CR-RC^2$  filter design illustrated in Fig. 7 was chosen. The default peaking time is 1  $\mu s$ , but it can be set to 0.5  $\mu s$  and 1.5  $\mu s$ . Longer peaking time values



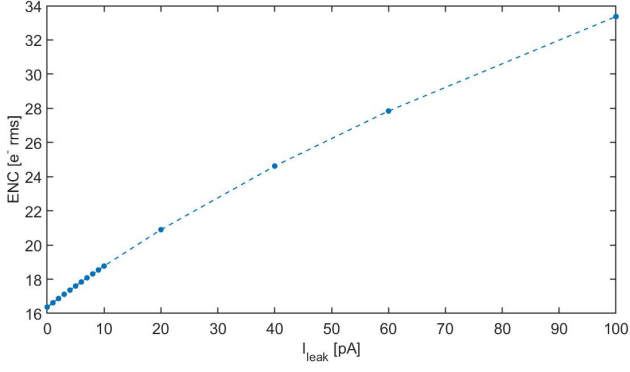


Fig. 6. ENC vs. detector leakage current ( $R_f$  not noisy,  $C_{det} = 1.5pF$ ).

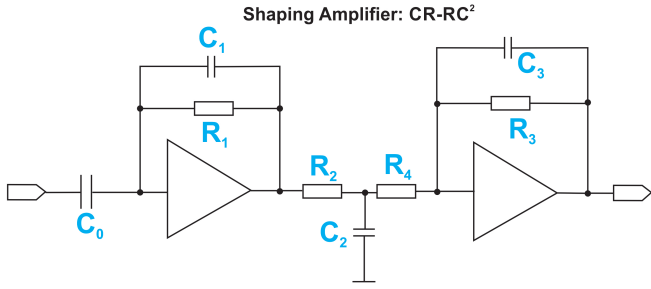


Fig. 7

do not improve the performance significantly and are also not preferable from the speed performance point of view.

The following stage is a base-line restoration circuit and a discriminator (Fig. 10) with a threshold set differentially and the bias current controlled by the 6-bit trimming digital-to-analog converters (DACs).

### III. READ-OUT ELECTRONICS OPERATING MODES

#### A. Basic performance with PZC

The first method to restore the base-line after the incoming hit is to use the Pole-Zero Cancellation circuit (PZC). The circuit comprises of the capacitance 10 pF and a MOS-based 50  $M\Omega$  resistance. The bias of the transistor in the CSA feedback and PZC circuit tracks the voltage shift at the CSA output to ensure proper feedback pole cancellation [10]. The comparison between the shaper output waveform without the PZC and with the PZC is shown in Fig. 8. Without the PZC the difference between initial base-line and the base-line after 500  $\mu s$  of equally distributed incoming hits (with 10  $\mu s$  period) rises to almost 30%.

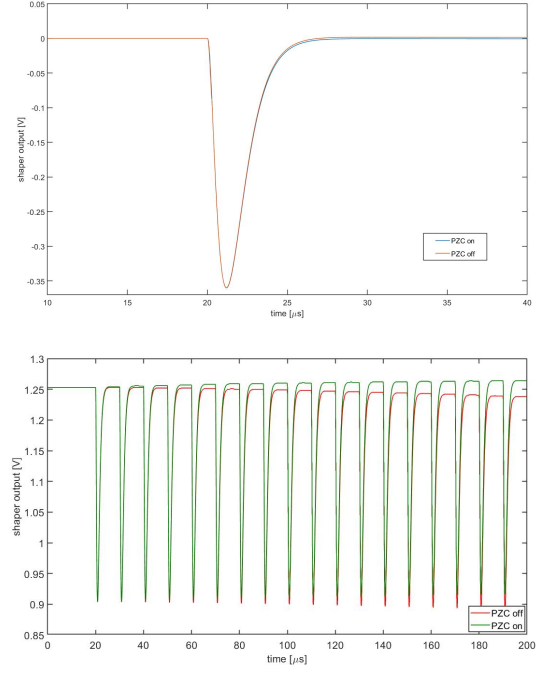
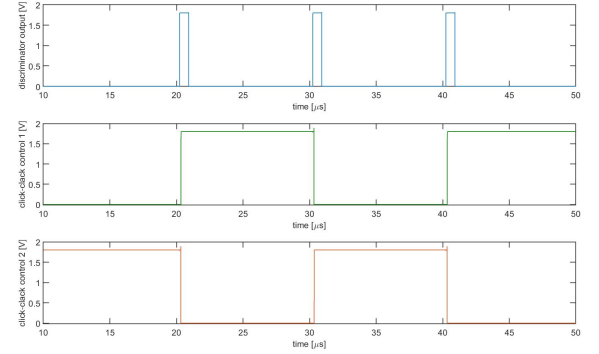
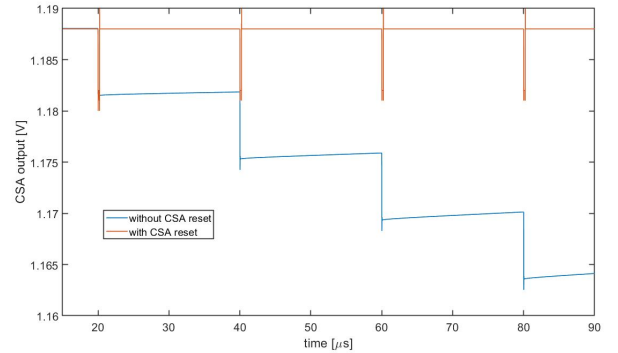


Fig. 8. Shaper output waveforms - pole-zero cancellation; a) single pulse, b) pulses train.

#### B. Active Feedback Discharge



(a)



(b)

Fig. 9. a) Control signals for Active Feedback Discharge circuit b) CSA output waveform without and with reset

Due to the large resistance in the CSA feedback the discharge time constant is also very long. That causes the DC voltage shift at the CSA output at high input count rates. To prevent the saturation of the CSA due to constant shift of the output voltage level, after each incoming pulse the CSA should be reset by discharging the feedback capacitor. The CSA reset is implemented by means of an Active Feedback Discharge (AFD) which means changing the polarity of half of the feedback capacitor [11]. The controlling signals (Fig. 9a) used to switch the capacitor are generated by the control logic using the discriminator output signal. The comparison of CSA output waveform without the reset and with the AFD [11] reset on is shown in Fig. 9b. The output voltage shift without the reset applied can be seen and actually it is significant.

### C. Base-line restoration circuit

The CSA reset works well for the fast baseline restoration at the CSA output but introduces an overshoot at the shaper output. To alleviate the problem we implemented base-line restoration (BLR) circuit that is triggered by the discriminator output [12]. The simplified schematic of the BLR is shown in Fig. 10. This circuit allows for fast reset of the shaper output and restoration of the baseline immediately after the peaking time of the shaper. The base-line restorer is implemented directly at the discriminator input.

The CSA output voltage with AFD reset turned on, the shaper output without the BLR, the discriminator pulses and shaper output with the BLR are shown in Fig. 11. The amount of overshoot can be controlled by the delay of the BLR control pulse after the discriminator rising edge.

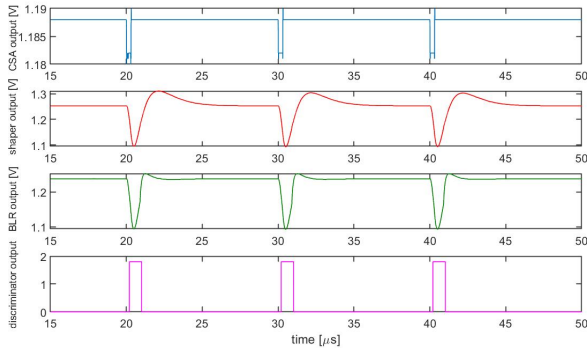


Fig. 11. Output waveforms, 1) CSA output, 2) shaper output, 3) discriminator output, 4) shaper output after base-line restorer.

The maximum achievable input hits frequency was simulated taking into account the discriminator response. The operation with PZC only can be used only for very slow input hit rates (several kcps) which is mostly due to the long CSA time constant ( $500\mu s$ ). For the mode of operation with the CSA reset only, the maximum frequency that can be reached does not exceed 750 kcps, whereas while using AFD reset and BLR simultaneously up to 1 MHz can be reached.

## IV. DESIGN IMPLEMENTATION

The design was implemented in 180 nm CMOS process on a die of  $1.5\mu m \times 3.2\mu m$  area. Apart from charge processing

channels it contains also biasing circuits and DACs and small area is occupied by another digital design from a separate project - see Fig. 13. The design was submitted for fabrication in Q3 2024.

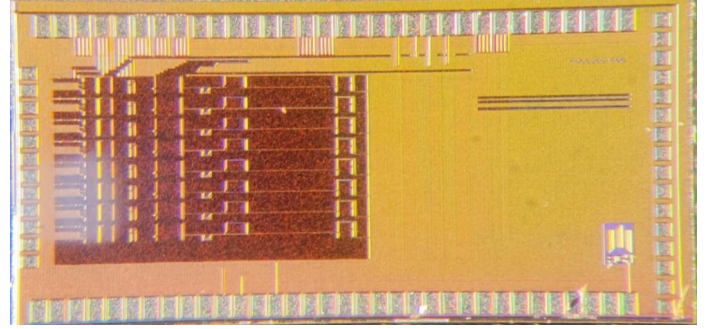


Fig. 12. The photo of the LNSTRIP ASIC.

The design was simulated using Monte Carlo and corner simulations to adjust the control range of the discriminator trimming DACs for PVT mismatch in the silicon. The output shaper amplitude and the differential discriminator input DC levels mismatch are presented in Fig. 14a and 14b respectively. The summary of the Monte Carlo simulations is shown in Tab. I.

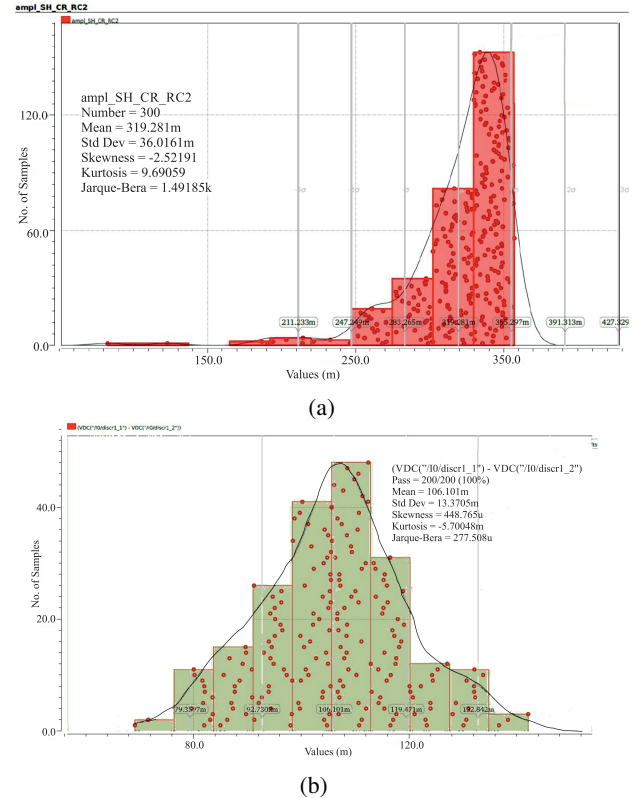


Fig. 14. Monte Carlo simulations of a) shaper output amplitude b) discriminator inputs differentially.

The shaper offset mismatch impact can be alleviated by the trimming DACs at the discriminator input. This allows to cover the range of 280 mV, what is much more than the discriminator differential inputs mismatch (Fig. 14b).

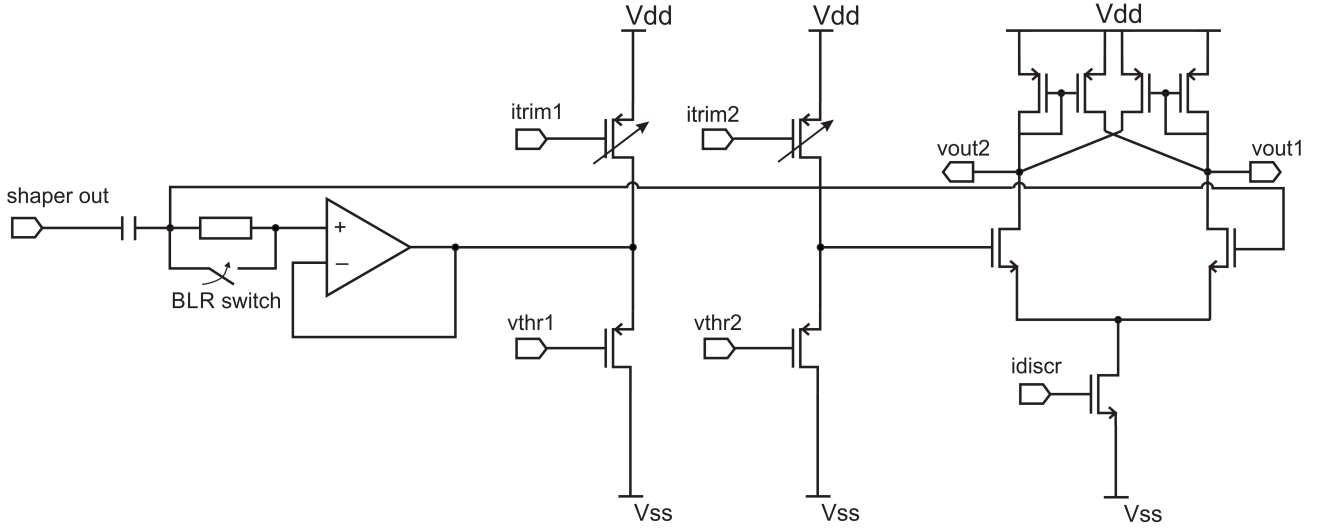


Fig. 10. Base-line restoration and discriminator circuit.

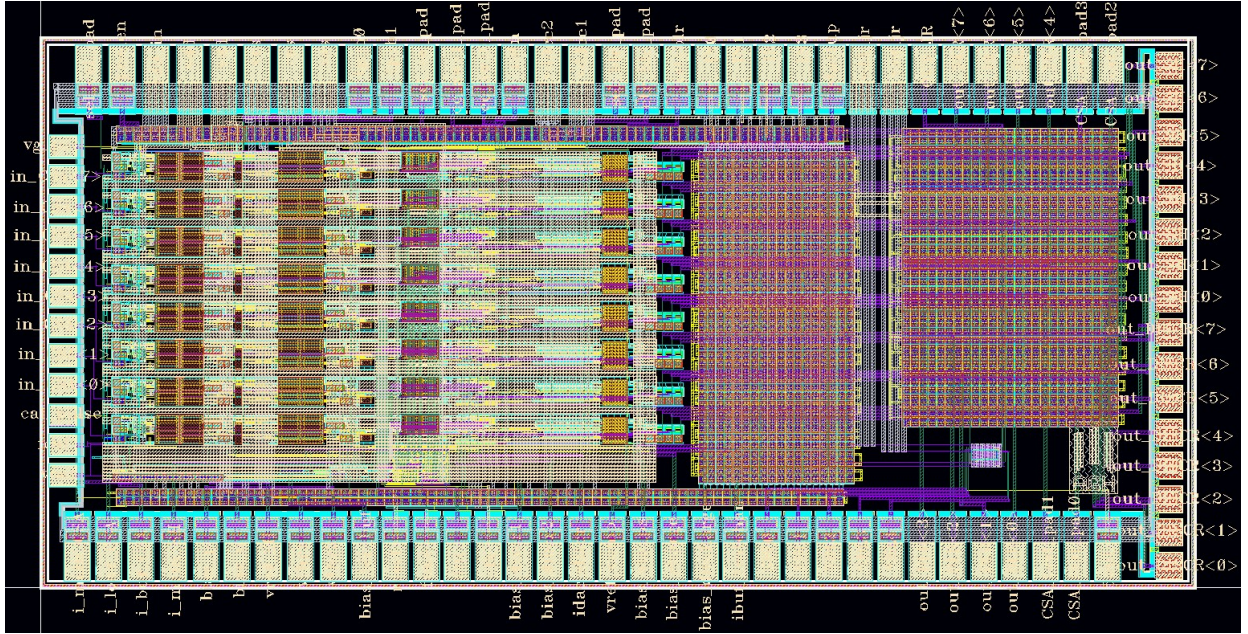


Fig. 13. The layout of the presented design.

TABLE I  
SUMMARY OF THE MC SIMULATIONS

|                       | Min   | Max  | Mean  | Median | Std   |
|-----------------------|-------|------|-------|--------|-------|
| ENC ( $e^- rms$ )     | 12.41 | 33.6 | 20.66 | 19.28  | 3.871 |
| CSA amplitude (mV)    | 6.1   | 7.31 | 7.06  | 7.16   | 0.235 |
| shaper amplitude (mV) | 240   | 378  | 345   | 351    | 25    |

According to the Tab. I the minimum achievable noise expressed as ENC is 12.4 electrons, mean value around 21 electrons, and the maximum around 34 electrons which is within acceptable range according to the design requirements.

The post-layout simulations revealed that the layout of the CSA reset circuitry is crucial for its proper performance and should be optimized carefully to minimize the coupling of the AFD control lines and CSA input/output signal lines. Fig. 15a shows the post-layout simulated CSA output without any

compensation. To get rid of the CSA base-line jumps, some major changes of the control lines layout were introduced. The post-layout simulated CSA output after optimization of the layout is shown in Fig. 15b. In this case the base-line jumps are not bigger than 0.3 mV, which is around 5% of the CSA amplitude for the default input charge value (2200 el.).

## V. CONCLUSIONS

In this paper an 8-channel prototype read-out electronics for silicon strip sensors was presented. The design was aimed to meet low noise requirements while allowing for high incoming hits rates. To achieve low noise all the noise contributors in the read-out circuit were taken into account. One of the trade-off was ensuring that the CSA feedback resistance is large enough not to compromise the noise performance, which on



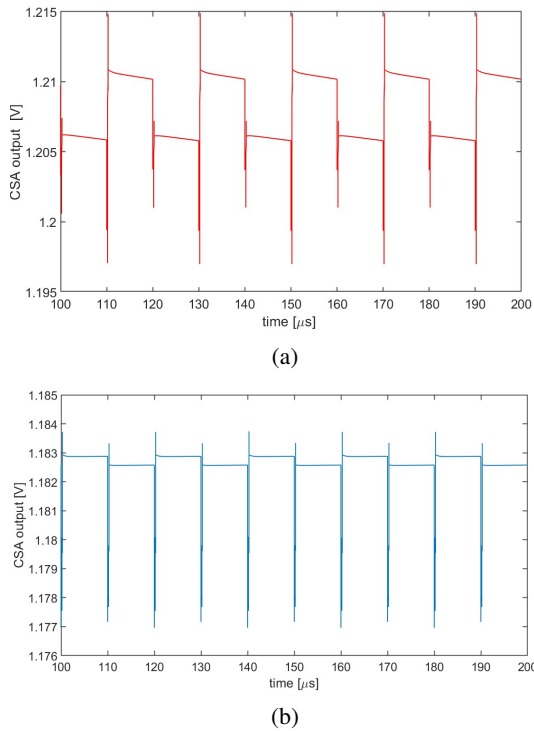


Fig. 15. Post-layout simulation of the CSA reset circuit a) layout without compensation; b) layout with compensation.

the other hand slows the circuit performance. Achieving the processing speed of few hundreds of kcps was possible by implementation of some digital techniques to support the baseline restoration and overshoot elimination after the CSA reset. The postlayout simulations results are promising and the chip was submitted for the tape-out in Q3 2024.

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