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FPGA Adaptive Predistorter Based on 64QAM Modulation

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***Abstract*—This paper presents a predistortion technique compensating for nonlinear distortions caused by HPA (High Power Amplifier) in a QAM (Multilevel Quadrature Modulation) system. Investigations were held both with software and hardware tools. It is confirmed by computer simulation that proposed approach produces a faster convergence speed than traditional computer performed algorithms. Predistortion technique based on programmable logic device is a very attractive from the implementation point of view, because of a low amount of required RAM and rapid convergence from a blind start.**

***Keywords*—Digital predistortion, HPA, FPGA, RF systems.**

I. Introduction

WIRELESS communications systems of the next generation are expected to provide its users with services that have information rates exceeding 2 Mbps. Supporting such high data rates with sufficient robustness to radio channel impairments requires careful selection of a modulation technique [1]. The Multilevel Quadrature Modulation (M-QAM) techniques such as 16-QAM or 64-QAM have a high spectral efficiency. This is a very attractive scheme of modulation for mobile communication or satellite transmission. But it is not suitable in practice because it is very sensitive to both AM/AM and AM/PM distortions introduced by the High Power Amplifier (HPA) [2]. The best way to compensate nonlinear distortions is linearization of the HPA by predistortion[3]. Predistortion is conceptually the simplest form of the linearization for a RF power amplifier. The predistorter distorts the input signal in such a way as to compensate for the nonlinear distortion introduced by the power amplifier. A fundamental advantage of RF predistortion is the ability to linearize the entire bandwidth of an amplifier or system simultaneously. It is therefore ideal for use in wideband multicarrier or systems, such as satellite amplifiers or in cellular base station applications [4], [5], [6]. We apply to our investigations digital predistortion structure with Look-Up Table (LUT), which is updated with the least mean square error algorithm . This table is used to correct the signal before feeding it to the HPA by the coefficient depending on the signal amplitude and phase. In this way the HPA nonlinearity can be compensated[7]. This paper is organized as follows. In Section II we examine system model in which we use the investigated predistorter. Section III is devoted to the detailed description of the adaptation algorithm used in it. Section IV describes the fundamental properties of a predistorted whereas section V gives an overview of an implementation into programmable logic device. Finally, in Section VI we present experimental results with our digital predistorter, which have been obtained for the QAM system. We conclude our paper with a discussion on simulation results.

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II. Performance of the QAM Modulation

Fig.1 shows the most common rectangular scheme of 32QAM, which has quaternary 8PAM transmission in I and Q. The standard form of rectangular QAM with M-array pulse trains is with M-array a_n^I and a_n^Q that is

$$s(t) = \sqrt{\frac{2E_S}{T}}\left[I(t)cos\omega_0 t - Q(t)sin\omega_0 t\right] \tag{1}$$

$$I(t) = c_0 \sum_n a_n^I \sqrt{T}\nu\left(t - nT\right) \tag{2}$$

$$Q(t) = c_0 \sum_n a_n^Q \sqrt{T}\nu\left(t - nT\right) \tag{3}$$

where $a_n^I, a_n^Q \in \{\pm(M-1), \pm(M-3), ..., \pm 1\}$

Here $\nu(t)$ is the usual orthonormal pulse and the transmission symbols are taken as odd integers. The latter is a common convention, which we adopt, but it does mean that a constant needs to be introduced in order to make $I(t)$ and $Q(t)$ satisfy the unit-energy normalization. This done, E_s becomes the QAM symbol energy, the average energy in one of the constellation points.

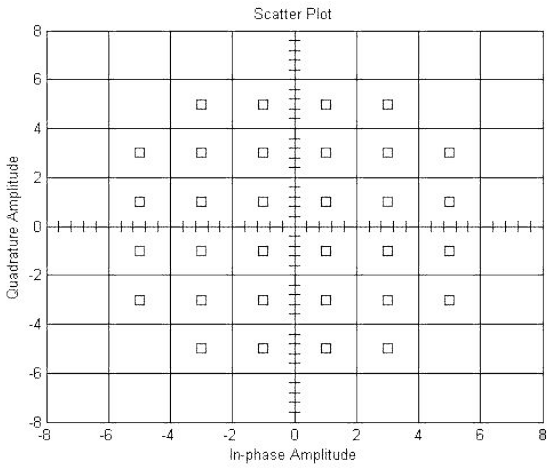


Fig. 1. Rectangular QAM constellation 32QAM. Values of a_n^I and a_n^Q are not normalized but are set to simple integers instead.

III. Behaviour of the Predistorter

In memoryless models, the output signal is assumed to be a nonlinear function of the instantaneous input signal only [8], [2], [9]. The envelope frequency of the input signal is much smaller than the envelope bandwidth of the amplifier. Consequently, the amount of amplitude and phase distortion depends only on the input signal level at the corresponding respective time instant. The equivalent scheme for the memoryless power amplifier behavioral model is shown in Fig.2.

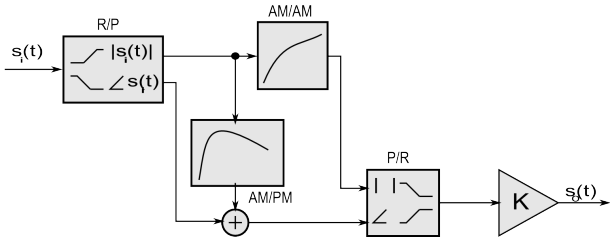


Fig. 2. Memoryless behavioral model of power amplifier.

In many practical simulations the behavior of memoryless HPA is characterized by its Amplitude to Amplitude conversion (AM/AM) and Amplitude to Phase conversion (AM/PM) [10]. These conversions are based on the Saleh [8] equations for real amplifier. The AM/AM parameters, α and β, are used to compute the amplitude gain for an input signal using the following function:

$$A(r) = \alpha_a \frac{r}{1 + \beta_a r^2} \tag{4}$$

where $\alpha_{a,\Phi}$ and $\beta_{a,\Phi}$ are constant parameters chosen to approximate Amplitude to Amplitude conversion and r is the envelop of the input signal. In order to compute the phase change for an input signal the following function is utilized:

$$\Phi(r) = \alpha_\Phi \frac{r^2}{1 + \beta_\Phi a r^2} \tag{5}$$

Fig. 3 shows typical plots for the Saleh method presenting output voltage against input voltage for the AM/AM conversion and output phase against input voltage for the AM/PM conversion.

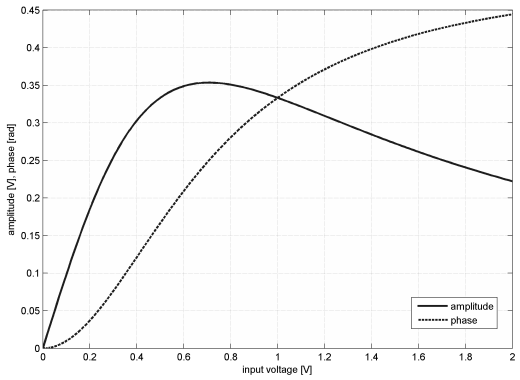


Fig. 3. Memoryless behaviour of the power amplifier. Example plots assuming $\alpha_{a,\Phi} = 1$ and $\beta_{a,\Phi} = 2$

Now let us examine the properties of the QAM with High Power Amplifier model defined with given numerical equations based on the Saleh method. We use memoryless behavioral model for our simulations. We assume that nonlinear distortions can be formulated in terms of AM/AM and AM/PM conversions and in the same manner as the amplifier distortion model. The envelope frequency of the input signal is much smaller than the envelope bandwidth of the amplifier. Consequently, the amount of amplitude and phase distortion depends only on the input signal level at the corresponding respective time instant [11], [12]. The equivalent scheme for the memoryless power amplifier behavioral model is shown in Fig. 2 [8], [2], [13].In this configuration we consider a quadrature modulated data sequence.

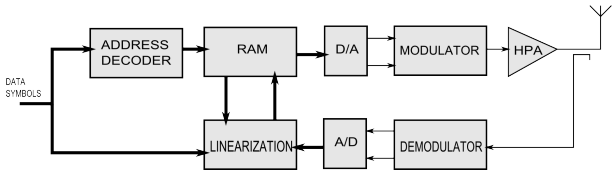
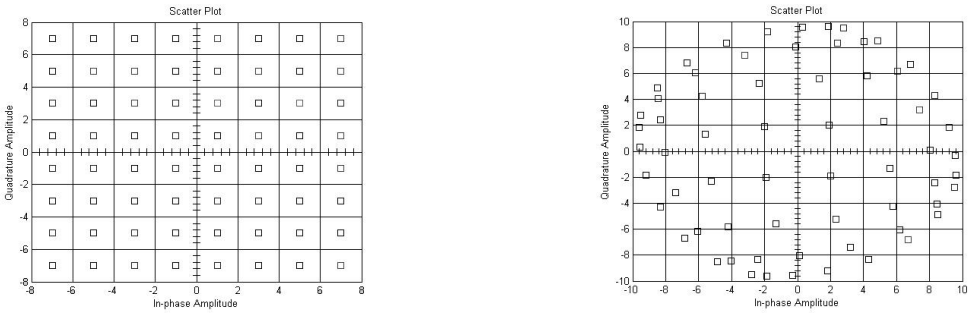


Fig. 4. Data symbols predistorter.

The predistorter distorts the input signal in such way as to compensate for the nonlinear distortion introduced by the power amplifier. Morover, predistorters may be designed to be adaptive. The adaptation property is a very desired feature because the characteristics of power amplifiers are time variant due to the temperature variation and aging [9], [14].

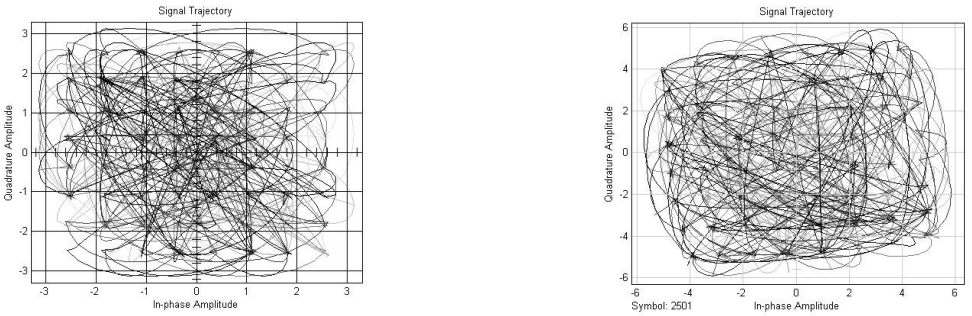
IV. Properties of Digital Predistortion

Fig.5 illustrates the amount of Bit Error Rate (BER) with linear amplifier. The 64QAM modulation is sensitive to nonlinearity of HPA, the amount of BER is high. Comparing Fig.5 (a) and (b), the amount of BER is very poor. This result enables the 64-QAM modulation scheme not be utilized in satellite communication systems without predistortion. It is clearly visible at Fig. 6 that power amplifier distortions warp the symbol constellation. Fig 6.a shows the signal constellation of the 64-QAM at the HPA input. Fig. 6.b shows the constellation of the 64-QAM at the HPA output. The influence on signal constellation of the power amplifier nonlinearites in more detailed manner is presented in Fig. 7 where we see trajectory constellations. The effect of nonlinear distortion can be evaluated also by the eyediagram of the system for output symbols. As it is seen in Fig. 8a, the eye-opening is much wider in the system with linear amplifier. In Fig.8b, the eye-diagram is illustrated, while the power amplifier is nonlinear, the eye is closing. Figure 9 presents the power spectral density of the 64QAM signal. In the QAM case, the PSD magnitude depends on the average signal amplitude. Curve (a) shows the power spectrum of the HPA output when linear amplifier is applied. Curve (b) shows distortions introduced by nonlinearities. It is clearly visible that the nonlinear distortions may decrase the bandwidth. After the power amplification the level of first side lobe in the transmited signal is about 20dB lower than the signal without it.



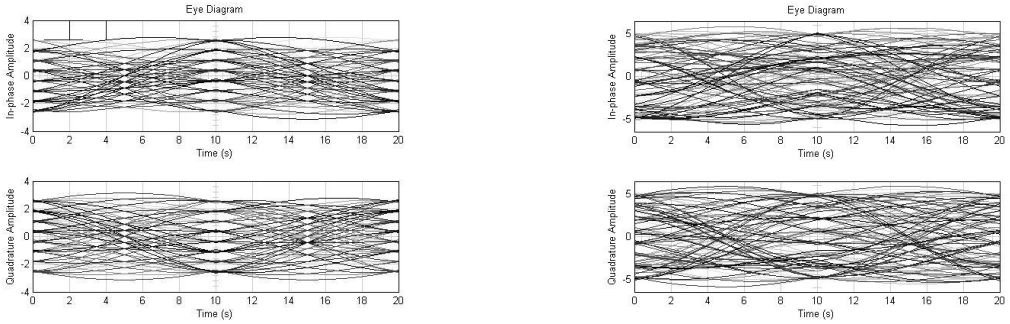
(a) undistorted (b) distorted

Fig. 6. Scatter constellations for 64QAM in Quadrature and In-Phase Amplitude.



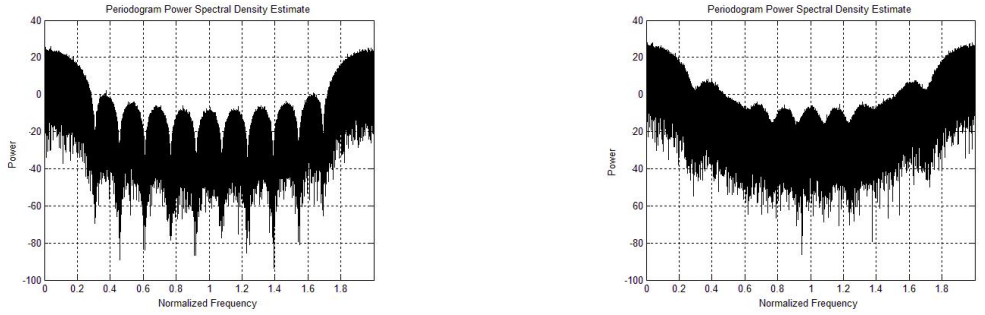
(a) undistorted (b) distorted

Fig. 7. Trajectory constellations for 64QAM in Quadrature and In-Phase Amplitude.



(a) undistorted (b) distorted

Fig. 8. Eyediagram for 64QAM in Quadrature and In-Phase Amplitude.



(a) undistorted (b) distorted

Fig. 9. Power Spectrum Density for 64QAM.

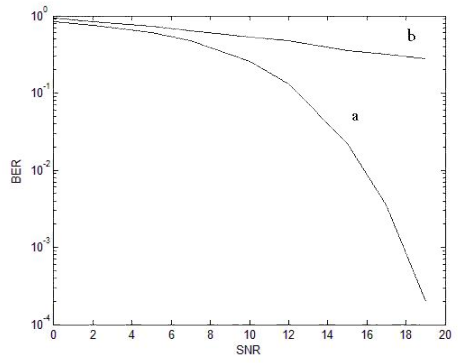


Fig. 5. Undistorted (a) and distorted (b) bit error rate for 64QAM.

V. HDL Implementation of Digital Predistorter

The predistortion idea may be easily implemented to meet the requirements of digital reconfigurable system composed of logic blocks described in the Hardware Description Language (HDL). Relatively low cost of prototyping and ease of making improvements makes the FPGA circuits an ideal mean to implement such a device in hardware [15]. The outlined scheme of the predistorter is presented in Fig. 10 Linearization block satisfies the functional equations [8]

$$ro_{RAM(qam)} = ro_{RAM(qam)} - \alpha(ro_i n - ro_{LUT(qam)}) \quad (6)$$

$$phi_{RAM(qam)} = phi_{RAM(qam)} - \beta(phi_i n - phi_{LUT(qam)}) \quad (7)$$

In the further considerations we will assume that scale factors α and β are

$$\alpha = \beta = 0.5 \quad (8)$$

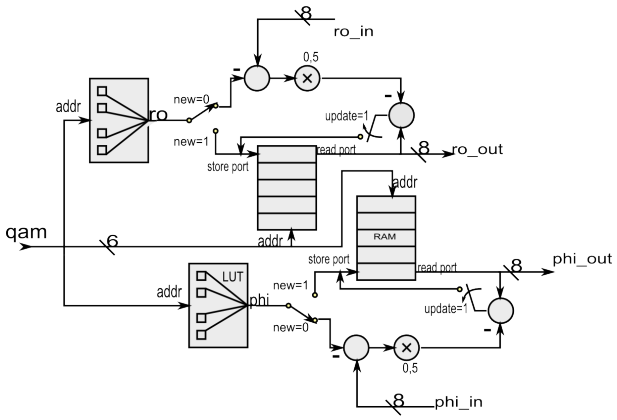


Fig. 10. Simplified diagram of the inner structure of a DP device.

The scatter constellations of QAM symbols may be decomposed into integer numbers each corresponding to the particular constellation point and thus acting as indices for transmitted symbols. The *qam* input vector has 6 bits for 64QAM and forms an address line for buffers used in the design. The addres chooses between all usable symbols in range $< 0; 63 >$. The QAM numbers are fed into the pair of Look-Up Tables (LUTs) in order to find the related polar coeffitients of *ro* and *phi* for the input. The Look-Up tables were implemented statically as robust combinational logic block to shorten the time of rectangular into polar conversion. The control logic of the block holds a separate Flip-Flop register to distinguish whether the input symbol was ever transmitted or not. If it wasn't - the *new* signal becomes active passing the input *ro* and *phi* into the storage RAM memories. After memory storage is complete - the symbol's *ro* and *phi* components are passed into the output. The RAM storing process may run in parallel with symbol transmission. This was however neglected in the implementation to ensure that the symbol was first stored properly. When the transmission occurs more than once for a particular symbol, *new* signal is inactive so the ouput is fed by RAM stored values. After sending a predistorted symbol's *ro_out* and *phi_out* values into the HPA the update process is needed in order to adjust the linearization block. The feedback signals of *ro_in* and *phi_in* are taken from the HPA's output and the *update* signal is set active to close the update loop.

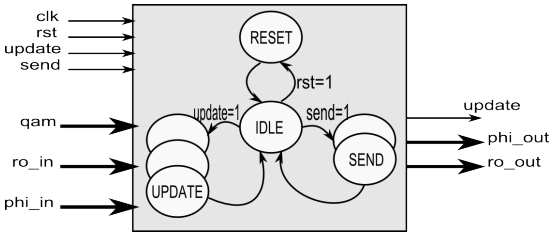


Fig. 11. Simplified block diagram of a predistorter device together with the FSM diagram.

The whole process is controlled sequentially with a Finite State Machine (FSM). This guarantees that all signals are driven with actual values and limits the block operation into a fixed set of clock ticks. The simplified block diagram of a predistorter device is presented in Fig. 11. For the substantial amount of time the device remains in *IDLE* state doing nothing and thus saving energy. The outcome for the last processed symbol is kept in output registers so there is no need to obtain it in any special way. There are two essential modes of operation First assumes the sending process in which the input symbol is translated into the predistorted one. The second mode assumes providing a feedback data and triggering the *update* signal. Additionally there is a *RESET* state provided causing the system to restore its initial state (setting DFFs to be sure that no symbols were ever transmitted).

VI. Simulation Results

Besides the Matlab modelling performed in order to investigate predistortion features described previously, some other simulations were made. That concerned two separate abstraction layers including *ModelSim* evaluation of a DP block described in VHDL and the hardware verification employing a PC computer linked with the FPGA board with a testing environment defined.

A. Modelsim Testing

For the functional testing of HDL blocks the ModelSim 6.4b Xilinx Edition was used. An abstract testing environment was developed for driving all essential input signals. The figure 12 shows an example output of the tested device. The LUT tables used for cartesian into polar conversion are performing a simple one-to-one translation. Thus, for testing the principle of operation the LUT cells may be filled with the same values as their adresses so the conversion doesn't affect the symbol. The input and output data is expressed as 8-bit signed values. The test case presented in Fig. 12 corresponds to the above convention. The input *qam* symbol is assigned with 2. After triggering the *send* signal for the first time the output turns into 2 as the update wasn't already performed and the LUTs are performing a selfsame conversion. In the next step the feedback values of *ro_in* and *phi_in* are set to 10 and the update is launched. This results in the following substitution

$$ro\_out = phi\_out = 2 - \frac{1}{2}(10 - 2) = 2 - 4 = -2 \qquad (9)$$

The next send strobe causes the device to transmit the RAM updated symbol. Performing any further update process with the fixed input values as stated above will make the subsequent decrease of the outcome by 4 in any iteration.

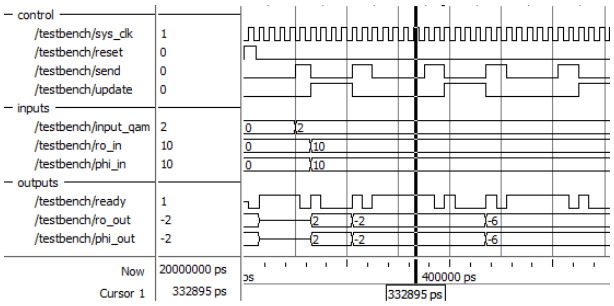


Fig. 12. Modelsim simulation waveforms while testing the digital predistorter.

B. Hardware Verification

In order to verify the digital predistorter it was synthesized into FPGA binary configuration file by Xilinx XST tool. A WebPack of 9.1 and 10.1 were used as development tools. As a target device the FPGA Spartan III XC3S500 was used together with a universal evaluation board holding all necessary peripherals. At the synthesis stage no special rules regarding speed or area optimization were applied. Table I summarizes the parametres of the synthesis.

TABLE I
FPGA DEVICE UTILIZATION REPORT

Parameter	value
Slice Flip-Flops	351
4 input LUTS	659
Occupied Slices	524
Logic LUTS	659
Route-through LUTS	92
32x1 RAM LUTS	64

It is worth to mention that the LUTs holding radius and angle values for corresponding QAM symbols were totally implemented in FPGA LUTs having only combinational logic. As the rectangular to polar conversion remains static - some optimization techniques regarding reduction of gate utilization may be applied to the design. The main goal of the hardware part was to implement a reconfigurable predistorter, thus in order to perform testing - some part of the testing environment was shifted into a PC computer software. The data exchange between PC set and the Digital Predistorter was carried out by a standard serial link employing RS232 hardware interface. Figure 13 summarizes the issue.

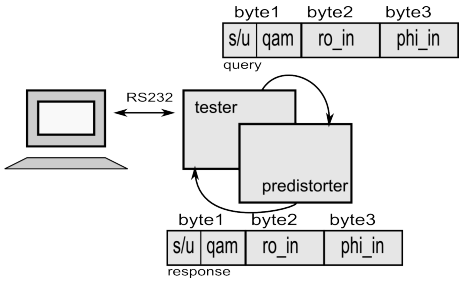


Fig. 13. Simplified diagram of Hardware testing set.

At the FPGA side an additional hardware was developed to deal with serial transmission and frame parsing. The data exchange is controlled by the PC in First-In-First-Out (FIFO) order according to request-response model. We assumed blocking communication so the PC won't perform any further action unless it will receive a response for the previous query. Frames have fixed length of 3 bytes. The first byte holds the *qam* symbol as well as the send/update bit (s/u). The PC software part was implemented in C++. Figure 14 shows the application's interface window. The program sends a frame containing the symbol to be transmitted. Then it acquires the ro_out, phi_out response from predistorter and computes HPA's response according to Saleh's model.

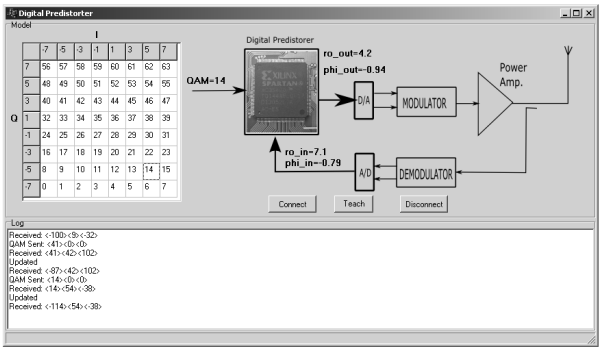


Fig. 14. PC testing application Interface

The response is then applied into the DP in another frame both with information triggering data update. In order to restore the system from the blind start a teaching procedure must be applied. This performs a teaching rounds by sending and updating all 64 symbols simultanously. This will make sure that the device will accomodate to the nonlinear characteristics of the HPA. Figure 15 shows the final predistorted

constellation for 64QAM after applying 20 teaching rounds into the device.

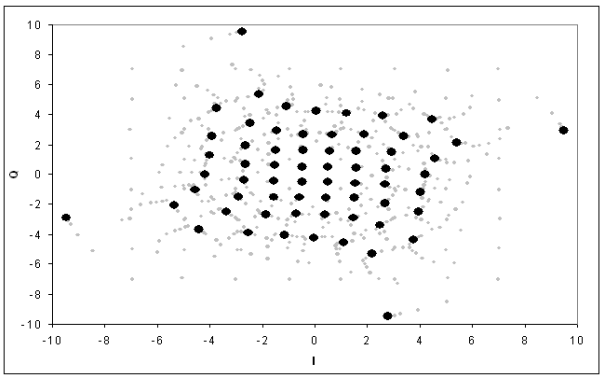


Fig. 15. Distorted 64QAM constellation obtained in 20 teaching rounds. The teaching convergence paths are marked with gray dots.

After teaching stage the predistortion device is ready to use. Figure 16 presents the output constellation for 64QAM transmitted by the non-linear HPA model with the digital predistortion. The predistortion was performed totally in hardware representing the radius and angle values with 8-bit precision. Responses acquired by the testing application were stored into textfile and plotted.

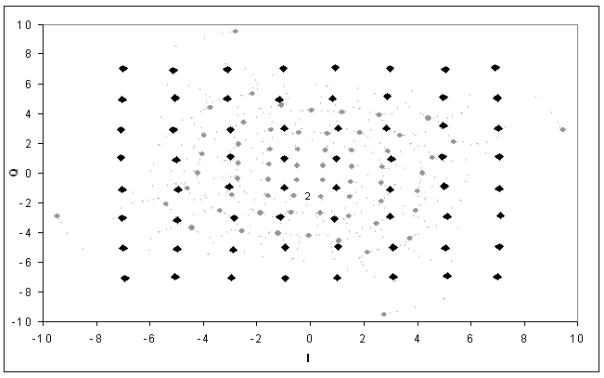


Fig. 16. Response of the HPA model with a predistorted constellation

VII. Conclusions

Digital data predistortion easily improves the linearity of HPA amplifiers. The general algorithm may be realized in hardware by using programmable logic. The example design was verified properly both with HDL testing environment as well as in post-synthesis by using the dedicated PC software with a serial link to the target FPGA device. The FPGA implementation utilizes low amount of resources and is fully scalable. The RAM and LUTs may thus be interchanged with an architecture tailored to the particular transmission scheme. The experiments proved that data predistortion can bring satisfactory results by using 8-bit data representation. The device after hardware implementation proved to have the ability of adaptation. The adaptation convergence makes the good accomodation in a few steps (typically about 10 teaching rounds for the whole set of symbols).

In our opinion, predistorter could be easily extended to other nonlinear parts of the RF circuits for computed modeling processes. In order to use this approach for other devices we need to do some measurements. From the simulation results, it is confirmed that the proposed pre-distorter with different IBO factor gives a good performance improvement of quality of the transmission compared to 64-QAM without it.

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