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Fast Determination of Similarity Between Two Vectors by Means of Analog CMOS Technique

Ryszard Wojtyna

***Abstract*—In this paper, an analog approach to determining a resemblance between two multidimensional vectors is proposed. As the resemblance measure, Euclidean distance is used. The main advantage of the presented method is a very high speed of the Euclidean–distance–measure calculations. The achieved high speed results from the fact that most of arithmetic operations needed to realize the calculations are carried out in parallel. This concerns the required operations of squaring a difference of two corresponding components of the compared vectors. Operating in a transconductane mode (voltage difference squaring transconductors) and a current mode (output square–root extracting circuit), our CMOS circuit is power saving. Its low–power operation results from the fact that sub–circuits of our calculator responsible for the squaring operations (a great number of them in case of large multidimensional vectors) consume no power in the absence of input signals. This takes place when corresponding components of the compared vectors are both equal to zero. The circuit also consumes a reasonably low amount of energy when processing (comparing) a different from zero input data (corresponding vector components). A simplified description of the applied differential squaring transconductors as well as the output current–mode square–root extraction circuit is given and a problem of good cooperation between them is discussed and proper solutions indicated. SPICE simulation results are shown to be in a good agreement with the theory presented.**

***Keywords*—Hardware signal processing, fast Euclidean distance calculation, analog CMOS circuits.**

I. Introduction

A NEED for fast determining similarity between two multidimensional vectors appears in many areas of signal processing nowadays. This concerns, among others, neural networks implemented in hardware [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], especially so–called self–organizing ones. One of important problems in such networks is how to learn them on silicon in a precise and fast way. New and attractive possibilities in this field offer methods that involve analog signal processing techniques. Competitive learning Kohonen networks based on WTA (Winner Takes All) and WTM (Winner Takes Most) methods [19] are well suited for this task, especially when applying current–mode circuits in a mixed–mode ASIC form (Application Specific Integrated Circuit).

In the WTA and WTM methods, the first step of the learning process is to determine a winner neuron that obtains a right to change its weights (WTA) or also weights of neurons belonging for some surrounding of the winner, which takes place in the WTM approach. Determination of the winner neuron is based on assessing similarity between an input vector of the network, X, and a weight vector, Y_j, associated with the j–th neuron [19]. As a similarity measure, Euclidean distance given by (1) can be used.

$$I_{OUT_j} = a\sqrt{b\sum_i \left(V_{X_i} - V_{Y_{ij}}\right)^2} \tag{1}$$

In (1), a and b are real valued coefficients, V_{X_i} a voltage at the i–th input node of the network, I_{OUT_j} a current characterizing the assessed similarity between X and Y_j, and $V_{Y_{ij}}$ a voltage representing a weight relating the i–th input node with the j–th output neuron. Summation of the $(V_{X_i} - V_{Y_{ij}})^2$ components can be easily preformed in hardware if they are converted to currents, because currents can be added in a single node, according to Kirchhoff's current law. This means that the voltage difference, $V_{X_i} - V_{Y_{ij}}$ after squaring should be transformed to a current form. Note that (1) can be expressed by means of two equations:

$$I_{O_{ij}} = b\left(V_{X_i} - V_{Y_{ij}}\right)^2 , \tag{2}$$

$$I_{OUT_j} = a\sqrt{\sum_i I_{O_{ij}}} . \tag{3}$$

From (2) it results that to perform the Euclidean distance calculation we need a differential transconductance squarer to realize this relation. In addition, we need a square–root–extraction (SQRE) circuit operating in a current mode to implement (3). As already mentioned, the current summation included in (3) can be easily carried out by connecting outputs of all differential squarers to one node, being the input of the SQRE current–mode circuit. This is illustrated in Fig. 1.

Quality of the Euclidean distance calculation performed according the scheme of Fig. 1 depends, first of all, on precision of the differential squaring and square–root–extraction operations. In [14] and [15], novel CMOS circuits suitable

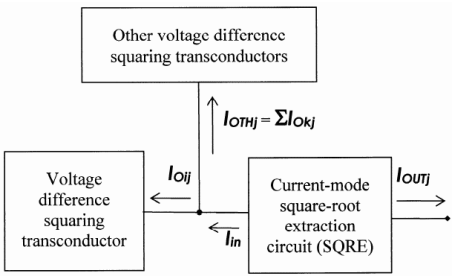

Fig. 1. Block diagram of the presented circuit for evaluating resemblance of multidimensional vectors.

R.Wojtyna is with the Faculty of Telecommunication and Electrical Engineering, University of Technology and Life Sciences, Kaliskiego 7, 85–796 Bydgoszcz, Poland (e-mail: woj@utp.edu.pl).

to realize these tasks have been proposed. Considerations presented in [14] and [15] concern separate operations of both circuits and do not take into account the influence of the SQRE circuit on the differential squarer. Two types of the squarers, noninverting and inverting ones were examined there. In each case, the obtained squaring precision was, unfortunately, not very good. In this paper, a selection of best solutions among those presented in [14], [15] and [16] have been made and some essential improvements in the circuit structure, designing and loading proposed. This has led to much better parameters of the obtained analog calculator.

The paper includes six sections. In section II, the voltage difference squaring transconductor is presented. Features of the SQRE circuit are described in section III. Section IV is devoted to the whole calculating circuit. Simulation results are given in section V, and concluding remarks in section VI.

II. Analog CMOS Circuit for Squaring Voltage Difference

Two CMOS circuits realizing the relation (2) have been proposed in [14]. They differ in the sign of the b coefficient in (2). For the circuit of Fig. 2, b is positive (noninverting transconductor) which means that the $I_{O_{ij}}$ current flows out from the squarer. For the other, Fig. 3, b is negative (inverting transconductor) and the $I_{O_{ij}}$ current flows into the squarer. Operation of both circuits is based on two differential pairs, M1–M2 and M3–M4, which are biased by drain currents of M5 and M6, respectively. In both circuits, transistors M11–M12 play a current mirror role and output current of the squaring circuits, $I_{O_{ij}}$, can be expressed by:

$$I_{O_{ij}} = I_{24} - I_{13} \ . \tag{4}$$

Denoting by I_{D5} drain current of M5 (tail current of the M1–M2 pair), by I_{D6} drain current of M6 (tail current of the M3–M4 pair), by i_{d5} differential current of M1 and M2 (current proportional to the $V_A - V_B$ difference) and by i_{d6} differential current of M3 and M4 (current proportional to the $V_A - V_B$ difference), I_{24} and I_{13} in (4) can be written as:

$$I_{24} = 0.5\,(I_{D6} + I_{D5}) + i_{d6} - i_{d5} \ , \tag{5}$$

$$I_{13} = 0.5\,(I_{D6} + I_{D5}) + i_{d5} - i_{d6} \ . \tag{6}$$

Taking (5) and (6) into account, (4) leads to:

$$I_{O_{ij}} = 2\,(i_{d6} - i_{d5}) \ . \tag{7}$$

For transistors operating in strong inversion and in saturation, their drain current is described by:

$$I_D \cong K\,(V_{GS} - V_{th})^2 \ , \tag{8}$$

where V_{GS} is gate to source voltage, V_{th} is threshold voltage and K a real valued coefficient.

Squaring properties on the circuits of Figs. 2 and 3 is achieved when the pairs M1–M2 and M3–M4 operate with small differential signals. From (8) we obtain the below given formulas describing transconductance gain coefficients, gm_{12}, gm_{34}, of the M1–M2 and the M3–M4 transistors, as functions of the input voltages V_X and V_Y:

$$gm_{12} = 2\sqrt{K}\sqrt{K_5}\,(V_X - V_{th}) \ , \tag{9}$$

$$gm_{34} = 2\sqrt{K}\sqrt{K_6}\,(V_Y - V_{th}) \ , \tag{10}$$

where the coefficient K concerns all the M1, M2, M3, M4 transistors of the differential pairs. K_5 and K_6 are related to the transistors M5 and M6, respectively.

Currents i_{d6}, i_{d5} in (7) depend on V_X and V_Y not only due to the transconductance gains given by (9) and (10), but also due to V_A dependence on V_X and V_B dependence on V_Y. The last two dependences are linear and have the form:

$$V_B = a_0 - a_1 V_Y \ , \tag{11}$$

$$V_A = a_0 - a_1 V_X \ , \tag{12}$$

where a_0 and a_1 are real–valued positive coefficients.

From (7) it is seen that the circuit output current, $I_{O_{ij}}$, takes different from zero values only when i_{d6} differs from i_{d5}, i.e. when the differences $V_B - V_A$ and, according to (11) and (12), $V_Y - V_X$ are different from zero (like in typical differential amplifier). Having in mind (9) and (10), i_{d6} and i_{d5} can be written as:

$$\begin{aligned} i_{d6} &= 0.5 gm_{34}(V_A - V_B) = \\ &= \sqrt{KK_6}\,(V_Y - V_{th})\,(V_A - V_B) \ , \end{aligned} \tag{13}$$

$$\begin{aligned} i_{d5} &= 0.5 gm_{12}(V_A - V_B) = \\ &= \sqrt{KK_5}\,(V_X - V_{th})\,(V_A - V_B) \ . \end{aligned} \tag{14}$$

Substituting (13) and (14) into (7), taking into account (11) and (12) and assuming $K_6 = K_5$, one obtains:

$$I_{O_{ij}} = 2a_1\sqrt{KK_5}\,(V_X - V_Y)^2 \ . \tag{15}$$

As already mentioned, (15) holds provided that conditions for small–signal operation of the differential pairs M1–M2 and M3–M4 are satisfied.

Output current, $I_{O_{ij}}$, of the noninverting squarer of Fig. 2, is allowed only to flow out from the circuit. This implies that transistors loading the squarer must be n-channel ones (NMOS), connected like shown in Fig. 2. There should be two of them because the circuit output voltage is higher than

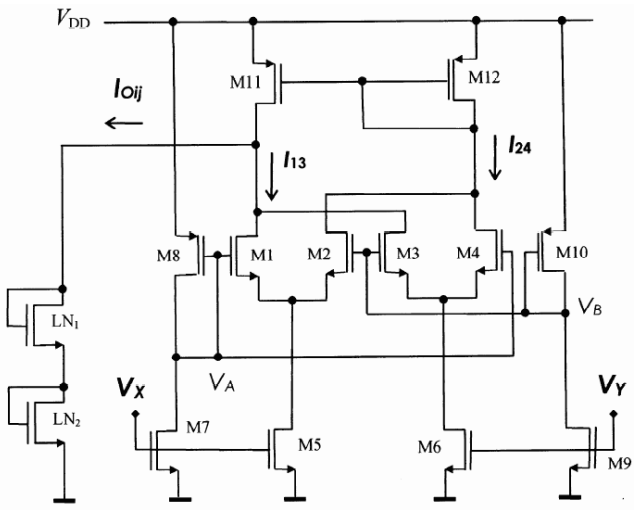

Fig. 2. Noninverting CMOS circuit for analog squaring voltage difference.

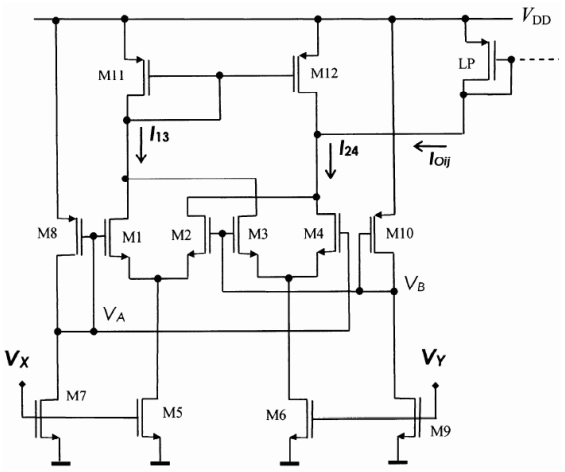

Fig. 3. Inverting CMOS circuit for analog squaring voltage difference.

one half of the V_{DD} supply voltage. This is a disadvantage of this solution. Another disadvantage is that reducing the V_{X_i} and $V_{Y_{ij}}$ voltages to a value below their threshold level may be insufficient do cut off the current consumed by the circuit and stop taking the supply power.

Unlike in the circuit of Fig. 2, the squarer shown in Fig. 3 enables the $I_{O_{ij}}$ output current to flow only into the circuit. As a result, a p-channel transistor (PMOS) with source terminal connected to the V_{DD} supply voltage source can be used as the squarer load. This solution is superior to that of Fig. 2 in two respects. First, only one transistor is required to load the squarer which allows us to ensure good conditions for the squarer operation. This is because the squarer output voltage is closer to the V_{DD} value than to the ground potential. Second, for the V_{X_i} and $V_{Y_{ij}}$ voltages being lower than threshold values of the used NMOS transistors (M5, M6, M7 and M9), no current is taken from the V_{DD} supply source, as the loading LP transistor is forced to be cut off as well. In [14] it was shown that the relation (2) also holds for the inverting squarer. Unlike in the previous squarer, a positive value of the output current, $I_{O_{ij}}$, means here a current flow into the squarer. The Euclidean distance calculator presented in section IV is based on squaring circuits of the type of Fig. 3.

III. Current–Mode Square Root Extracting CMOS Circuit

To realize to operation described by (3), a current mode circuit shown in Fig. 4 was used. It serves as the required square root finder (SQRE) and has been proposed in [15]. Its output current is denoted by I_{OUT_j} and input one is a sum of $I_{O_{ij}}$ currents delivered by the voltage difference squaring transconductors operating in parallel, according to (3). This circuit can be loaded by an NMOS transistor (LN) or a PMOS one (PN), as I_{OUT_j} can flow in both directions. The case with the LN load is better because then the SQRE output voltage, V_o, is lower and enables to increase the circuit dynamic (wider range of the current variations). This is because the dynamic is restricted by the $V_{DD} - V_o$ voltage difference.

In Fig. 4, the tail current of the M1–M2 differential pair, I_t, representing the sum of I_1 and I_2 currents, is linearly related

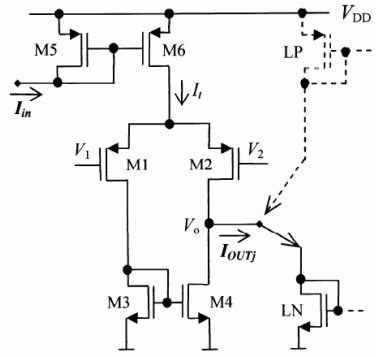

Fig. 4. Analog CMOS current–mode square–root–extraction circuit (SQRE).

to the input current, I_{in}, which can be written as:

$$I_1 + I_2 = kI_{in} \ , \tag{16}$$

where k is a positive coefficient, and I_1 and I_2 are drain currents of the M1 and M2 transistors, respectively, operating in strong inversion and in saturation. This allows us to write:

$$I_1 \cong K\left(V_1 - V_S - V_{th}\right)^2 \ , \tag{17}$$

$$I_2 \cong K\left(V_2 - V_S - V_{th}\right)^2 \ , \tag{18}$$

where V_{th} is the transistor threshold voltage and V_S source potential of the M1–M2 differential–pair transistors.

Output current of the circuit is given by:

$$I_{OUT_j} = I_2 - I_1 \ . \tag{19}$$

Solving the set of equations (16)–(19) with respect to I_{OUT_j} we obtain:

$$I_{OUT_j} = \left(V_1 - V_2\right)\sqrt{2kK}\sqrt{I_{in} - \frac{K}{2k}\left(V_1 - V_2\right)^2} \ . \tag{20}$$

Because only positive values of I_{OUT_j} are allowed, due to the n-channel LN transistor that can conduct current only in one direction, V_1 cannot be lower than V_2. For small signal operation, i.e. when the following condition holds:

$$I_{in} >> \frac{K}{2k}\left(V_1 - V_2\right)^2 \ , \tag{21}$$

(20) simplifies to the form:

$$I_{OUT_j} \cong \left(V_1 - V_2\right)\sqrt{2kK}\sqrt{I_{in}} \ . \tag{22}$$

As can be seen from (22), output current, I_{OUT_j}, of the circuit shown in Fig. 4 is proportional to square root of its input current I_{in}. Thus, the circuit is a current–mode rooter.

IV. Low–Power Low–Voltage CMOS Circuit for Fast Assessing Vector Resemblance

A full electrical scheme of the proposed Euclidean distance calculator is shown in Fig. 5, where only one squaring transconductor is shown in details for simplicity reasons. Transistors realizing the transconductor are numbered from 1 to 12, while transistors used in the SQRE finder numbered from 21 to 26. The LN transistor is the circuit load. Transistor M25, being an input transistor of the SQRE circuit, is the load of the parallel connected squaring transconductors. If the

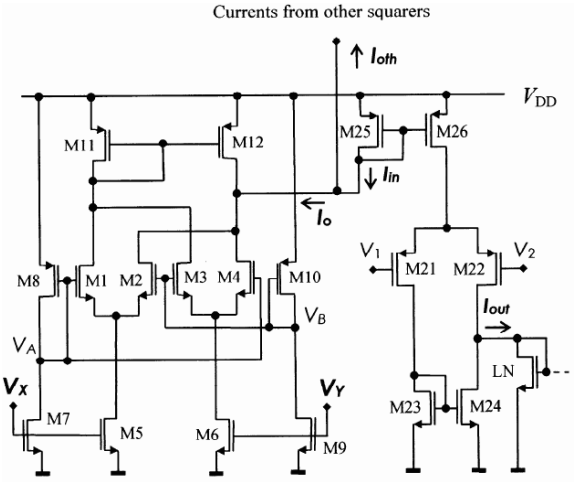

Fig. 5. Low–voltage low–power analog CMOS circuit for very fast vector resemblance evaluation.

input voltages, V_{X_i} and $V_{Y_{ij}}$, drop below threshold voltages of the NMOS transistors, the total supply current becomes zero. This is an advantage and means power saving. As will be seen in the next section, the V_{DD} supply voltage, for which the calculator operates with a high precision in a wide range of input and output signal variations, is low compared to the threshold voltage values. The V_{DD} voltage being roughly twice as high as the value of sum of NMOS and PMOS threshold voltages (sum of absolute values) is sufficient to obtain a good performance of the proposed analog calculator.

V. Simulation Results

To verify the expected good properties of the proposed circuits, SPICE simulations were carried out for the supply voltage equal to $V_{DD} = 2.5V$. Threshold voltages were $V_{thn} = 0.4655V$ and $V_{thp} = -0.617V$ for NMOS and PMOS transistors, respectively. Figures 6–8 concern the inverting squaring transconductor of Fig. 3, for which the load is simpler than for the noninverting one and creates better condition for power–saving operation. Input voltages, V_{X_i} and $V_{Y_{ij}}$, were changed in the range from 0 to $2.5V$. Transistor sizes for this circuit are given in Table I.

Fig. 6 shows output current, $I_{O_{ij}}$, as a function of the $V_{X_i} - V_{Y_{ij}}$ input voltage difference (white markers). V_{X_i} was varied from 0 to $2.5V$ for a constant value of $V_{Y_{ij}} = 1.25V$. To assess precision of the squaring operation, first and second derivatives of $I_{O_{ij}}$ with respect to V_{X_i} as functions of V_{X_i} are shown in the middle and upper plots, respectively. For ideal squaring, the function representing the first derivative should be linear and the one representing the second derivative constant. From the middle and upper plots one can note that the squaring operation is precise for V_{X_i} ranging from about $0.75V$ to $1.75V$. The same can be observed from the bottom plot in Fig. 7, where apart from the transconductor characteristic (white markers) also an ideal mathematical quadratic function is shown for comparison reasons. A good similarity between both curves is visible even for a wider input–voltage range, i.e. for V_{X_i} varying from $0.5V$ to $2V$. This range amounts 60% of the supply voltage value ($V_{DD} = 2.5V$),

TABLE I
Channel Width (W) and Length (L) of Transistors Included in the Circuit of Fig. 3

	Transistors						
	M1	M2	M3	M4	M5	M6	M7
$W[\mu m]$	2.5	2.5	2.5	2.5	0.4	0.4	0.4
$L[\mu m]$	0.6	0.6	0.6	0.6	33	33	55
	Transistors						
	M8	M9	M10	M11	M12	LP	
$W[\mu m]$	50	0.4	50	2	2	2	
$L[\mu m]$	0.35	55	0.35	0.5	0.5	0.5	

which is a good result. In other words, effectiveness of utilizing the supply voltage is not bad.

In the top plot of Fig. 7 we have drain–source voltages of two PMOS transistors, M11 and M12, which make up the output current mirror of the transconductor. The point is that values of these voltages should be similar and their changes should be small in order to avoid so called channel–length modulation effect. This is one of necessary conditions for precise operation of the mirror and, as a consequence, precise operation of the squarer. As can be seen from the upper plot in Fig. 7, the difference between these voltages is acceptably small over the considered input voltage range.

Fig. 8 presents current taken from the supply voltage source (curve marked by white squares) and power dissipated by the transconductor (marked by black squares) as functions of the V_{X_i} input voltage, for $V_{Y_{ij}}$ being constant. The power curve is a product of the white marked curve (actual value of the current) and $V_{DD} = 2.5V$. Both curves do not approach zero when V_{X_i} goes to zero because $V_{Y_{ij}}$ is higher than threshold voltage of the NMOS transistors. Otherwise, both traces would go to zero for V_{X_i} approaching zero. In other words, this

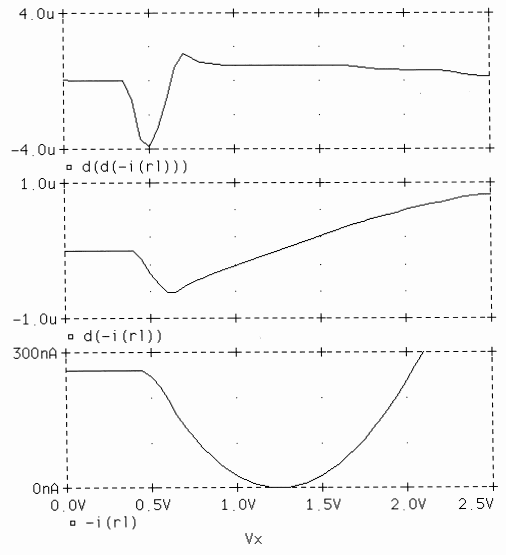

Fig. 6. Transfer characteristics of the squaring transconductor of Fig. 3: a) output current, $I_{O_{ij}}$, versus V_{X_i} for $V_{Y_{ij}} = 1.25V$ (bottom), b) first derivative of $I_{O_{ij}}$ with respect to V_{X_i} versus V_{X_i} for $V_{Y_{ij}} = 1.25V$ (middle), second derivative of $I_{O_{ij}}$ with respect to V_{X_i} versus V_{X_i} for $V_{Y_{ij}} = 1.25V$ (upper).

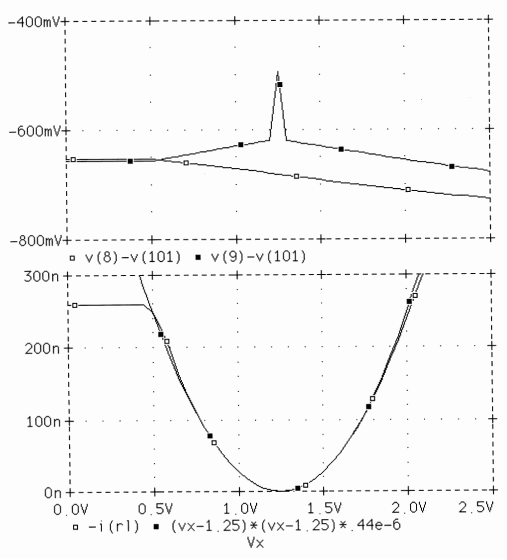

Fig. 7. DC properties of the squaring transconductor of Fig. 3: a) output current, $I_{O_{ij}}$, versus V_{X_i} for $V_{Y_{ij}} = 1.25V$ (bottom plot, white markers), b) mathematical quadratic function $y = 1.25(V_{X_i} - V_{Y_{ij}})^2$ (bottom plot, black markers), c) gate–source voltage of M11 (upper plot, white markers), d) gate–source voltage of M12 (upper plot, black markers).

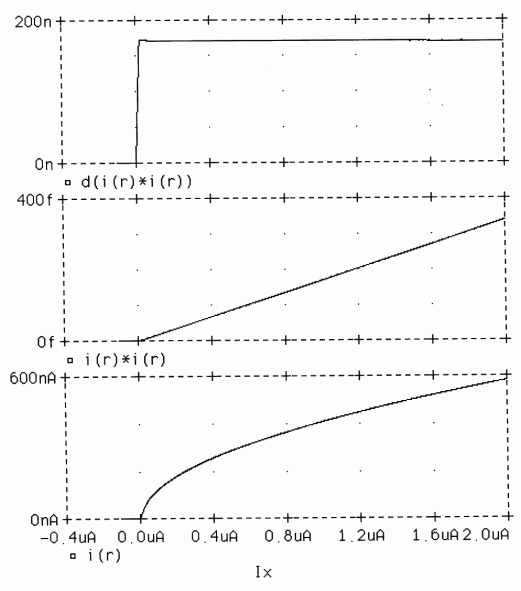

Fig. 9. DC transfer characteristics of the SQRE circuit of Fig. 4: a) output current, I_{OUT_j}, versus the input current I_{in} bottom plot, b) output current square, $I^2_{OUT_j}$, versus the input current I_{in} middle plot, c) $d(I^2_{OUT_j})/dI_{in}$ derivative versus the input current I_{in} upper plot.

figure does not show one of the important advantages of the squaring transconductor, namely that it consumes no power when being inactive. This is only a picture for an active state of the transconductor. Over the input voltage range where the squaring precision is acceptably high (from $0.5V$ to $1.5V$), the consumed power is less than $13\mu W$, which is a good result.

Simulation results concerning the square root finder (SQRE circuit) of Fig. 4 are presented in Figures 9 and 10. Sizes of transistors engaged in building this circuit are gathered in Table II and differ from that presented in [15] significantly. The transistor numbers in Table II are exactly like shown in Fig. 3, but are different from transistor numbers used in Fig. 5 to indicate the SQRE circuit. In case of Fig. 5, these numbers have been generated by adding 20 to numbers from Table II. This is because in the full calculator of Fig. 5, with both the squaring transconductor and the SQRE circuit, no number can be used twice.

Voltages controlling the SQRE current gain are equal to $V_1 = 0.88V$ and $V_2 = 1V$. In comparison to the values given in [15], ($V_1 = 0.98V$ and $V_2 = 1V$), the circuit presented in this paper exhibits a much lower sensitivity of the circuit current gain to variations in the control voltages (six times lower), which is an advantage. This has been reached mainly due to changes in transistor sizes. These changes have also lead to improvements in other circuit parameters like precision and power consumption. In Fig. 9, transfer properties of the SQRE circuit are presented. The bottom plot shows output current (I_{OUT_j}) as a function of the input one (I_{in}). A square root extraction character of this curve is clearly seen. To enable assessing accuracy of the root extraction operation, square of the output current ($I^2_{OUT_j}$) versus the I_{in} current has been shown in the middle plot and a derivative of the output current square with respect to I_{in}, i.e. $d(I^2_{OUT_j})/dI_{in}$, as a function of I_{in} is given in the upper plot.

For an ideal square root extraction, the output current square

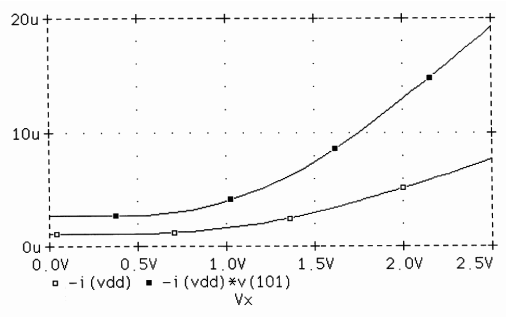

Fig. 8. Current (marked by white squares) and power (denoted by black squarers) consumed by the squaring transconductor of Fig. 3.

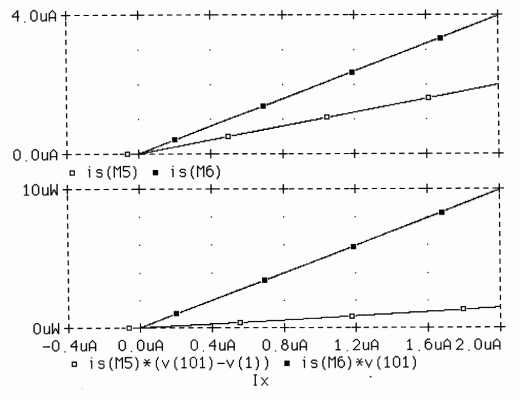

Fig. 10. Currents (upper) and power (bottom) consumptions in the SQRE circuit of Fig. 4 as functions of I_{in}: a) consumption due to the I_{in} current white squares, b) consumption due to the I_t current black squares.

TABLE II
CHANNEL WIDTH (W) AND LENGTH (L) OF ALL TRANSISTORS CREATING THE SQUARE ROOT FINDER OF FIG. 4

	Transistors						
	M1	M2	M3	M4	M5	M6	LN
$W[\mu m]$	0.6	0.6	0.6	0.6	2	4	0.6
$L[\mu m]$	6	6	1.6	1.6	0.5	0.5	1

$(I^2_{OUT_j})$ should be linearly dependent on the input one I_{in}. From the middle plot and especially from the upper one it is seen that this relation is highly linear for the input current ranging from about $20nA$ to about $2\mu A$. Thus, dynamic of the output current variations, expressed as a ratio of its maximum do minimum values, amounts 100 and is higher than that achieved in the circuit presented in [15] and [16].

A low–power operation of the SQRE circuit is shown in Fig. 10. The bottom plot presents power and the upper current consumptions as functions of the input I_{in} current. Note that the supply current as well as the consumed power are increasing functions of I_{in} and equal zero if I_{in} is equal to or less than zero. This is an important advantage of the SQRE extracting circuit and means no power consumption in the absence of input current, with no other efforts. This has been reached, among others, due to loading the circuit in the way shown in Fig. 4, i.e. by means of a grounded NMOS transistor that plays a role of the I_{OUT_j} receiver.

The curves denoted in Fig. 10 by white squares concern the input M5 transistor and the others refer to the rest of the circuit, connected with the supply V_{DD} source by means of the transistor M6. It is seen that the supply current and the power consumed by the M5 transistor are lower than that consumed by the remaining part of the circuit. This is the price we pay for achieving high precision and wide range of the SQRE output current variations. Total power consumption of the circuit is a sum of the powers represented by the curves shown in the bottom plot. As can be seen, the level of power consumed by the proposed SQRE circuit is acceptably low when operating with low currents.

VI. CONCLUSIONS

A problem of fast Euclidean distance calculations useful to assess similarity between two large multidimensional vectors was considered in this paper. New possibilities in solving this problem offer analog techniques based on CMOS technology. Two CMOS circuits enabling calculation of the Euclidean distance similarity measure were presented.

One circuit is a transconductor squaring a difference of two voltages. These voltages, denoted in Fig. 5 by V_{X_i} and $V_{Y_{ij}}$, represent corresponding components of the compared vectors, whose similarity is to be evaluated. The Euclidean–distance calculator of Fig. 5 includes several operating in parallel squaring transconductors of Fig. 3. The parallel operation of them is the main reason why the whole circuit of Fig. 5 can work very fast even if the multidimensional vectors are large (important advantage of the proposed circuit). The other module in the calculator of Fig. 5 is a current mode circuit suitable to perform a square root extraction (SQRE) on the sum of currents delivered from the squaring transconductors. The proposed Euclidean distance calculator is attractive, among others, to be used in competitive learning self–organizing networks by means of WTA (Winner Takes All) or WTM (Winner Takes Most) training method. A lot of place in this paper has been devoted to the problem of achieving a good cooperation between the squarer and the SQRE circuit and increasing precision of the squaring operations. This has been reached by improving circuit schemes, modifying transistor sizes and ensuring proper currents flowing through the MOS transistors included. As a result, the presented calculator is a fast, precise and power–saving circuit, attractive for signal processing in hardware.

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