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Application of Digital Control Techniques for Satellite Medium Power DC-DC Converters

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***Abstract*—The objective of this paper is to present a work concerning a digital control loop system for satellite medium power DC-DC converters that is done in Space Research Centre. The whole control process of a described power converter is based on a high speed digital signal processing. The paper presents a development of a FPGA digital controller for voltage and current mode stabilization that was implemented using VHDL. The described controllers are based on a classical digital PID controller. The converter used for testing is a 200 kHz, 750W buck converter with 50V/15A output. A high resolution digital PWM approach is presented. Additionally a simple and effective solution of filtering of an analog-to-digital converter output is presented.**

***Keywords*—DC-DC switching converter, digital feedback loop, FPGA, VHDL, digital current-mode control, digital voltage regulator, bang-bang control, digital PID, DPWM.**

I. Introduction

DIGITAL control of a power converter in space applications has several advantages over the traditional analog devices. Some effects having a significant influence on a long time performance of a controller include aging of elements, single event effects (SEE) and total ionizing dose (TID). The aging means that parameters of controller parts change as the time passes thus modifying frequency response and possibly stability margins. The same applies to TID. SEE can cause transient or even latch-up in controller reducing performance and reliability of a converter. In analog controllers nothing can be done to compensate these changes after design phase. Those effects have to be taken into account at the beginning of a design by leaving margins large enough to keep the system stable during the whole mission. In digital controller parameters of the compensator stay constant regardless of time or irradiation. If it is required, a digital control gives a possibility to update controller's coefficients to new values. It is also much easier to implement a redundancy that can help avoid SEE that can lead to abnormal behavior of the system. Such a redundancy cannot be easily implemented in analog controller and usually requires duplicating whole converter. In digital domain redundancy can be achieved by duplicating only essential parts of controller or implementing "triple vote" technique. A digital signal processing also allows extending the redundancy by implementing error detection and correction codes.

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There are numbers of structures that can be used to implement a standard PID controller. Solution presented in this paper is based on an ideal-parallel structure. It was used to stabilize the system in voltage mode. A mathematical description of a system shows how this model can be used to evaluate an influence of compensator coefficients to the system response before applying them to a real device. Frequency response plots of a physically realized system are presented.

Apart from a voltage mode it is possible to use a current mode control in a DC-DC buck converter. The control of the system in this mode is more complex than in a voltage mode. The current mode control solution used in presented controller is shown.

II. General Model

The outline block diagram of a digital buck converter used for described design is shown in Fig. 1. An analog part of a typical buck converter consists of inductance L, capacitor C at the output and two transistors Q_1 and Q_2. The control-to-output transfer function of an open-loop system in voltage mode is as follow:

$$G(s) = \frac{V_0(s)}{D(s)} = \\ = \frac{R(CR_C s + 1)}{CL(R + R_C)s^2 + C(RR_C + RR_L + R_C R_L)s + (R + R_L)} \quad (1)$$

where: R is load, C is capacitor at the output, L is inductance, R_C is parasitic resistance (ESR) in the capacitor and R_L is a parasitic resistance in the inductor.

If output voltage of the DC/DC converter is outside the range of the analogue-to-digital converter then resistor divider should be added and the above equation should be updated by multiplying by proper transfer function of the divider.

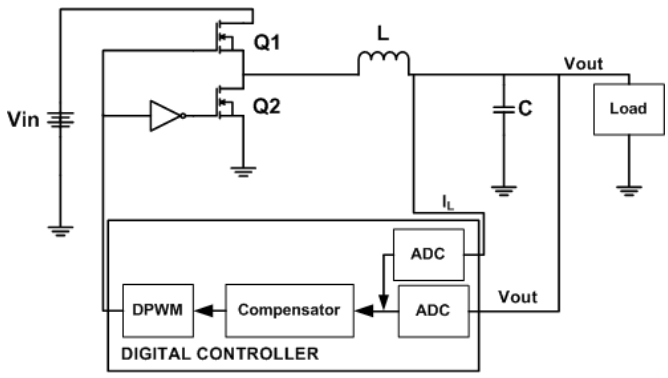

Fig. 1. Block diagram of a buck converter.

The digital part of a typical buck converter presented in Fig. 1 consists of four main parts: two ADCs – analog-to-digital converters, compensator and DPWM – digital pulse width modulation. The lower ADC measures the output voltage, eight times per one switching period, giving the result as 12 bit width positive value. The upper ADC measures the inductor current three times per switching period. The compensator part is a controller that calculates the control effort to keep the output voltage at desired level. The controller is described in more details below. The last block is a digital implementation of a standard PWM. The main task of this element is to switch on and off the switching transistors Q_1 and Q_2 at moments calculated by a controller.

The controllers that were used in the implementation of the converter were decided to be PID in two different implementations, a bang-bang controller (for overvoltage protection tests) and 50% duty controller. The 50% controller always sets the duty ratio equal to 50% regardless of the load. The controller of this kind is needed during a start of converter in the voltage mode to avoid a full-time opened transistor Q_1 in absence of soft-start circuit. The bang-bang is a controller that acts as rockets in table tennis that bounce a ball. When the output voltage is below the given value the controller switches on the transistor Q_1 and switches off the transistor Q_2. If the voltage is above the given value, the controller makes the opposite, so it switches off the transistor Q_1 and switches on the transistor Q_2. The final controller that was implemented was a well known PID controller. Its implementation in details is given in section IV.

Proposed current mode solution is based on replicating operation principles of analogue current mode controllers in digital domain. In analogue current mode controllers voltage error is amplified and filtered in error amplifier and then compared to inductor current value. When signal proportional to inductor current becomes higher than amplified voltage error, transistor is turned off. In most cases additional correction ramp has to be summed with inductor current slope, to stabilise the controller.

Digital implementation of current mode is based on the same operation scheme. Voltage error is filtered and passed to the PID controller. Resulting control is then compared to the current ramp. Because current cannot be sampled fast enough to provide sufficient time resolution, current ramp has to be recreated inside the controller using few closely spaced samples at the beginning of the current ramp. Those samples (two in this case) are used to estimate current ramp slope and level. Additional correction ramp is added by adding user-defined slope and level values to those calculated in previous step. After parameters are calculated, the ramp is recreated by multiplying counter value with calculated slope value and adding calculated level. The counter is update at a rate of 100 MHz giving 100 MSPS current slope equivalent. Each sample of the recreated ramp is then compared to output of PID controller. At the moment when ramp becomes higher than PID output, DPWM is disabled thus turning off the transistor.

III. Hardware

The chosen hardware used for the test system is Xilinx Spartan-3 XC3S1500 on board the Altium's Nanoboard 2. The power stage controlled by FPGA is medium power (750 W) buck DC/DC converter supplied by EADS Astrium. Two 12 bits LTC2366 analog to digital converters on custom made PCBs were used. Additional driver and current measurement circuits were built to interface nanoboard to DC/DC converter.

IV. Implementation

The logical block diagram of the implemented system is presented in Fig. 2. In the following paragraphs all of the blocks are described.

The *Reset* module is responsible for a switching on/off and resetting the system in a predictable way to avoid putting random values to the DPWM during the initialization, the module keeps switched off modules like: AI, ADC, filter and reference as long as necessary to initialize them. After that the DPWM is allowed to be turned on.

The *ADC* module measures the voltage level at the output and converts it to a 12 bits width digital value. Read-out is done every 0,625 μs (8 times per one switching cycle). The oversampling is done to allow making a simple filtering. For example during a standard readout there can occur some transients or disturbances. These can follow in a wrong estimation of an error and bad applied control effort. The oversampling is also very important in failure or overvoltage conditions. While measuring the output voltage it is possible to detect the overvoltage condition and automatically turn off Q_1 transistor protecting the load.

The *Filter* module is capable of making linear or non-linear filtering on the digital input voltage value. The oversampling allows basic filtering as calculating the mean value of the output voltage in this case. A non-linear filtering is done by median filter. The filtering of the measured voltage value makes the controller less susceptible to noise.

The *Reference* module calculates the error between desired voltage level and the real voltage at the output of the converter. The desired output voltage level can be set by user in real time using user interface (UI) module.

The *Bang-bang* controller module as its name suggests is responsible for using bang-bang principle for keeping the voltage output level about the desired value. The module every 0,625 μs takes the error value from Reference module and if the error is smaller than zero it forces the Q_1 transistor to be off and Q_2 to be on. If the error is bigger than zero then transistor

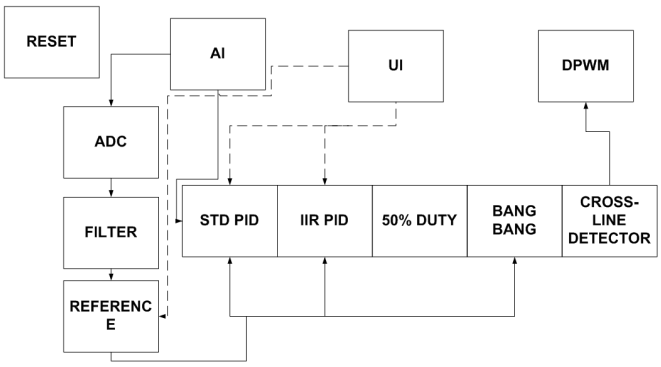

Fig. 2. Logical representation of the implemented system.

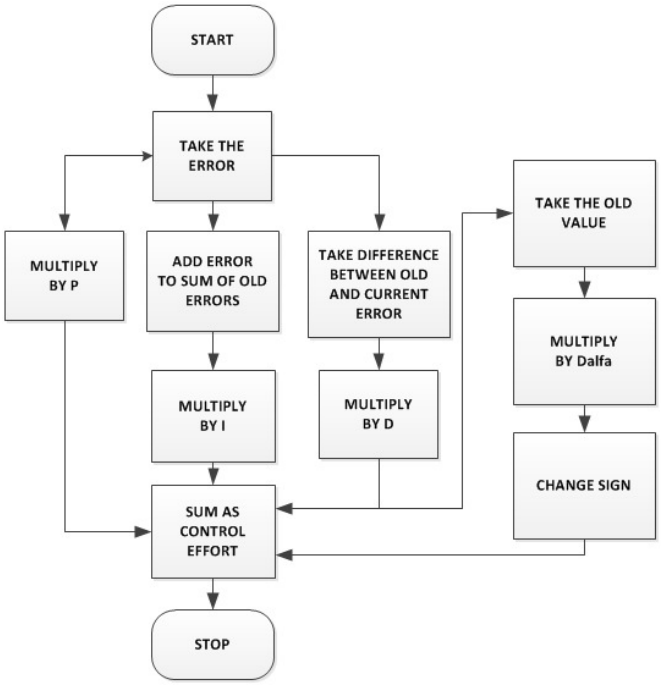

Fig. 3. Block diagram of a Std. PID implementation.

Q_1 is forced to be on and Q_2 to be off. The module was used in our case to test the possibility to digitally protect the whole system against the overvoltage or under-voltage conditions.

The *50% duty cycle* module generates control effort of the 50% duty cycle. The module can be used to test the whole system – checking if the power stage works correctly. The second task of this module is limiting duty cycle during start-up of a converter. Without dedicated soft-start circuit voltage mode PID controller generates large positive overshoot during start-up when switched on with 0 output voltage. This voltage spike can trigger overvoltage protection in electronic load that is used to test the converter. It can be overcome by powering up the converter with 50% duty cycle controller and then switching to regular PID. That way overshoot is significantly smaller and does not trigger overvoltage protection in electronic load.

The *Std. PID* and the *IIR PID* are two modules that implement the PID using two different approaches. A PID can be coded in digital domain using several different ways. We decided to use two of them. The first one is to use "algorithmic" approach. In this case we can formulate the PID as the algorithm shown in Fig. 3.

The presented standard algorithm can be very often met in implementations in higher level languages like C/C++ or Java. In the first step latest error value is calculated. Then it is multiplied by P coefficient and the result is kept in memory. Simultaneously latest error is added to the sum of all previous errors – it can be treated as integration. Afterward the result is multiplied by I coefficient and the product is also kept in a memory. Parallel to both above operations a difference between the current error value and the error from the previous cycle is calculated – this corresponds to getting a derivative. The difference is then multiplied by D parameter. Additionally previous value of the product of D and error derivative is calculated, then it is multiplied by Dalfa coefficient and its sign is changed to opposite – this can be regarded as adding a pole in high frequencies. After all above calculations are finished they are added together and result with a control effort that after scaling to a 0 to 1 range can be applied to the DPWM.

The second approach bases on the general digital PID formula below:

$$D(z) = \frac{a_0 + a_1 z^{-1} + a_2 z^{-2}}{1 + b_1 z^{-1} + b_2 z^{-2}} \tag{2}$$

The equation can be implemented using four different so called direct implementations. Due to simplicity and good understanding so called 3D implementation was used.

The *UI (User Interface)* module is responsible for interaction between the system and the user. The module gives the possibility to the user to set up desired voltage level, P, I, D and Dalfa coefficients in Std. implementation of the PID controller. It is also possible to set up the a_0, a_1, a_2, b_0, b_1 and b_2 parameters in IIR PID implementation. Additionally a user can "switch off" desired bits (replace them with 0) that come from ADCs to check the influence of ADC noise to the overall performance of the system. All the changes made by the user are applied in real-time and they do not require restarting the digital control loop.

The *AI (Artificial Intelligence)* unit is a core of the system. It sends requests to different modules of the system to make new measurements, calculate error, perform filtering and/or calculate PID control effort. AI is a unit that synchronizes the other modules to make them work in correct order.

The *DPWM* module is a simple digital implementation of a PWM generator. The DPWM consists of a counter that resets the output to a low level when the counter value is equal or higher than a given value that comes from a currently selected controller. The same happens when Cross-line Detector detects that current slope is higher than error voltage (in current mode). After the counter reaches its maximum, the counter is set to zero and the output is set to high level.

ADC for current mode is a unit that controls the analog to digital converter for making measurements of the actual current. The module makes three measurements in the first half of the switching cycle. The measurements are correlated with voltage readouts and occur at the same time instants. The correlation is necessary due to high noise that is introduced to the system by ADCs.

Cross-line Detector is responsible for estimating when the current slope will cross the calculated control value. There are two measurements during the on-time in a current switching period. These two measurements allow estimating the slope of the current ramp (a) and its magnitude (b) during the first and/or second measurement. Additionally we generate an artificial ramp (a_c) to keep the controller stable.

$$y(x) = (a + a_c) * x + (b + b_c) \tag{3}$$

The calculated parameters are then summed together with correction ramp a_c and b_c that ensure the stability of the system (according to theorem of current mode stability conditions). Equation (3) describes the calculation described above. Coefficients a_c and b_c can be set by the user.

V. Test Setup

To make the basic set of different measurements there was created an automatic test stand. The test stand consists of the following devices:

- *Oscilloscope: Tektronix MSO 4054*
- *Riddley Frequency Response Analyser*
- *Power Supply: E3631A*
- *Power Supply: Agilent 6675A*
- *Electronic Load: Agilent N3300A*
- *National Instruments PXI with LabVIEW Environment*

Additionally for some tests and debugging Logic Analyser TLA5201 paired with Oscilloscope Tektronix DPO7104 were used.

Four tests with different input voltages and output currents were performed:

- *Static measurement input/output measurements (input current, input voltage, output current, output voltage)*
- *Load step response (200W 2A to 600W 12A step)*
- *Open loop frequency response*
- *Audiosusceptibility*

Static measurements were performed using load and power supply readout capability. Load step response was measured by triggering all electronic load channels to switch at one moment and recording output voltage with oscilloscope. Open loop frequency response was measured with frequency response analyzer by injecting signal from generator to control loop input and measuring output voltage. For audio-susceptibility measurement, signal injecting circuit was connected between input voltage source and power converter. Signal on input voltage was injected and measured on input and output with frequency response analyzer.

To perform all presented below tests all instruments were connected via USB or GPIB with PXI chassis with controller and controllers for each device were written in LabVIEW. Afterwards, the controllers were set together and a final program for performing all tests was created. Additionally a report generator unit was added.

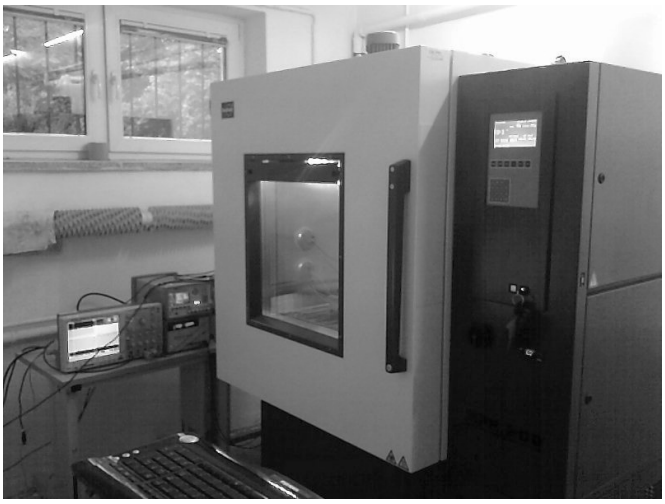

Fig. 4. Climate chamber KPK200.

TABLE I
PID Parameters for Voltage Mode

Parameter:	Hexadecimal value:	Value that should be used in time simulation:
P	0x04500	4.3125
I	0x00600	$7.32421875*10^{4}$
D	0x0ff00	$8.16*10^{-6}$
Dalfa	0x00200	0.125

TABLE II
PID Parameters for Voltage Loop in Current Mode

Parameter:	Hexadecimal value:	Value that should be used in time simulation:
P	0x0c500	12.3125
I	0x01500	$2.5634765625*10^{5}$
D	0x0ff00	$8.16*10^{-6}$
Dalfa	0x00200	0.125

Both converters: an analog and digital one, were set and tested using one template of tests. The tests was performed for load current values of 15 A, 12 A, 8 A, 2 A, 0.5 A with input voltages 60 V, 70 V and 80 V.

The PID parameters for voltage mode were constant over the all bench tests, and are shown in Table I.

The PID parameters for voltage-loop in current-mode were also constant over the whole bench tests, and are shown in Table II. Compensation ramp value was set to: 0x880 (0.53125) or 0x680 (0.40625). It should be noted that the time of the current cross line with reference that was got from PID was shifted once to the left in measurements in high input voltages.

The tests for a thermal chamber were made also using above given parameters. To change the temperature we used KPK 200 (Fig. 4).

All the equipment used in the tests on the bench was placed near the climate chamber. Since FPGA board could not be placed inside the chamber driver and ADCs wires had to be routed outside the chamber. It required longer wires that affected converter performance. The same tests as previously performed on bench were repeated, but without audio-susceptibility. Test sequence was repeated under 4 different temperatures: 0°C, 20°C, 40°C, 60°C. The converter was tested only in those temperatures, because components added to the converter i.e. drivers and parts of current sensing circuit were not specified for operation in military or industrial temperature ranges. Temperatures were chosen to give the impression of what changes in operation can be expected and not to fully qualify the device.

VI. Results

All the open loop frequency response plots that are shown below include inverting error amplifier, thus phase plots are shifted by 180° from conventional Bode plots.

A. Voltage Mode Results

On digital voltage mode converter frequency response charts it can be seen that there is about 7 kHz of gain bandwidth with

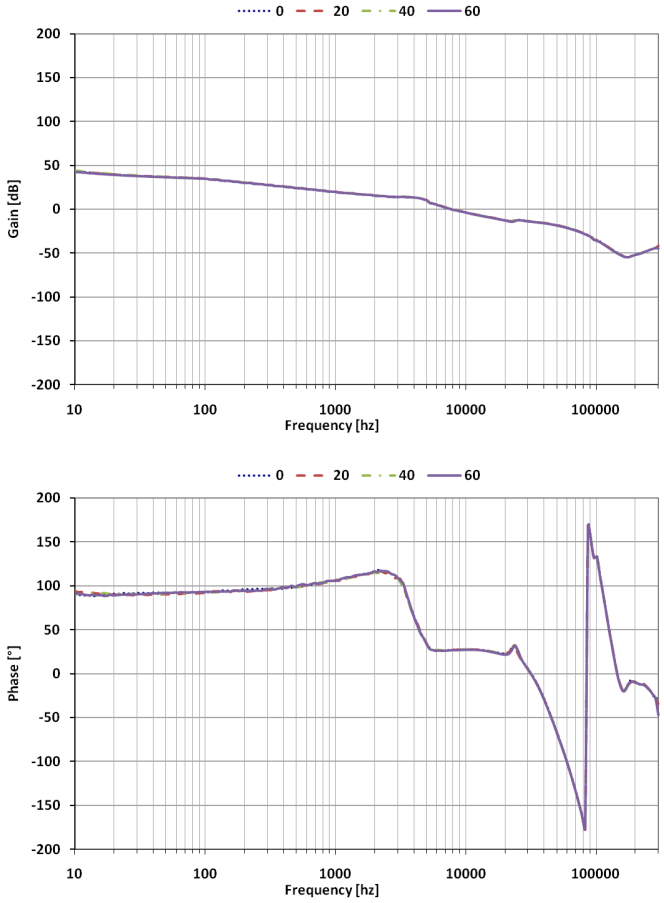

Fig. 5. Voltage mode frequency response.

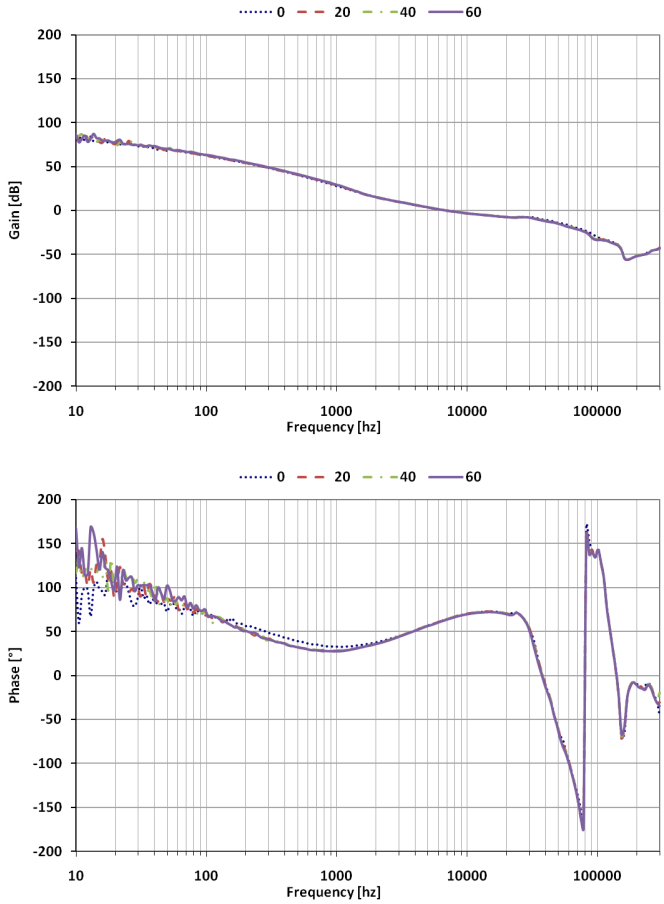

Fig. 7. Current mode frequency response.

30° phase margin and 15 dB gain margin (see Fig. 5.). These parameters remain consistent for low load currents. At higher loads phase margin drops to 15°.

Digital converter frequency response phase decreases rapidly after 20 kHz. It can be explained by a delay between taking measurement and applying control effort (turning the switch off). In presented implementation the delay varies between 2 μs and 4 μs (there is also some influence of digital filter). Such a delay reflects closely the decrease in phase observed in digital converter. That delay cannot be completely removed and is inherent in digital control. It can be mitigated by changing the time when measurement is taken and control effort is calculated.

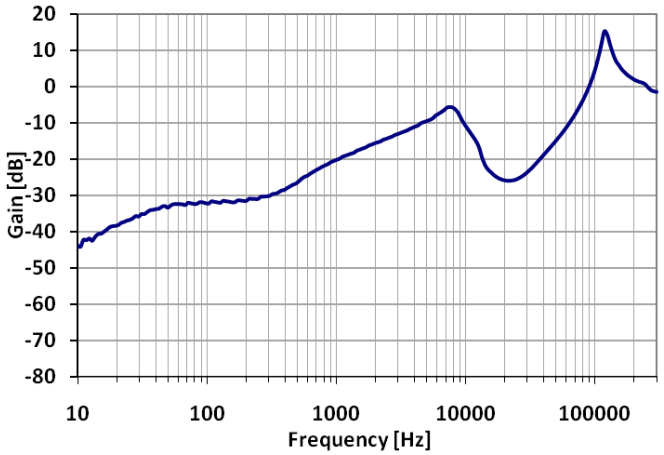

Fig. 6. Voltage mode audio-susceptibility.

The input ripple rejection, also called audio-susceptibility of the digital voltage mode converter is shown in Fig. 6. The figure reveals that the system's feedback loop attenuates a signal that is injected into the converter starting from around 40 dB in low frequencies decreasing to around 5 dB about 7 kHz.

B. Current Mode Results

Bandwidth of the digital converter is about 7 kHz with 60° phase margin and 12 dB gain margin (see Fig. 7). These parameters are constant through all measurements except discontinuous current mode, where bandwidth decreases to around 5 kHz.

Other features specific to the digital implementation are similar with those mentioned in previous section.

The audio-susceptibility of the digital current mode converter is given in Fig. 8. The analysis of the figure shows that the system's feedback loop attenuates a signal that is injected into the converter starting from around 80 dB in low frequencies decreasing to around 30 dB about 7 kHz. This result is much better if compared to digital voltage controller.

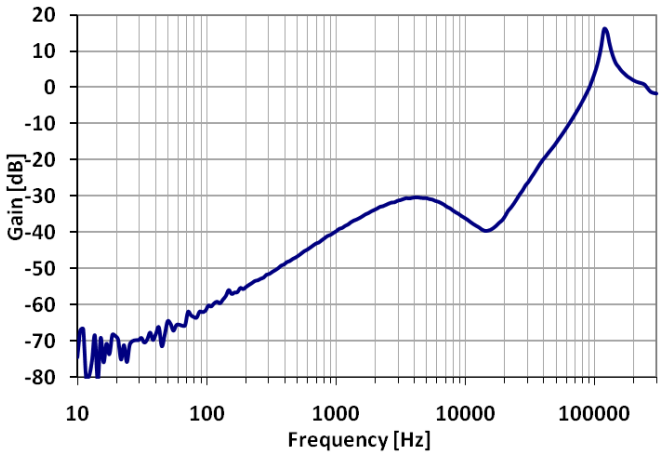

Fig. 8. Current mode audio-susceptibility.

An example of a step response of the converter is shown in Fig. 9. During the step in the load the output voltage drops rapidly by around 4 V followed later by around 1 V overshoot. After the overshoot the system goes back without any additional oscillations to the requested output voltage. The time needed for the system to complete recover the output voltage is around 1ms.

C. Thermal Results

Climate chamber measurements show that analog and digital frequency characteristics do not change much (see Fig. 5 and 7). There are visible variations in phase and gain of digital converter in voltage and current mode at low frequencies. That phenomenon is due to problems with long wires and ground connections.

D. Other Results – Quantization of ADC, Overvoltage Protection

An example of an overvoltage protection behavior is presented in Fig. 10. It is possible to detect the overvoltage

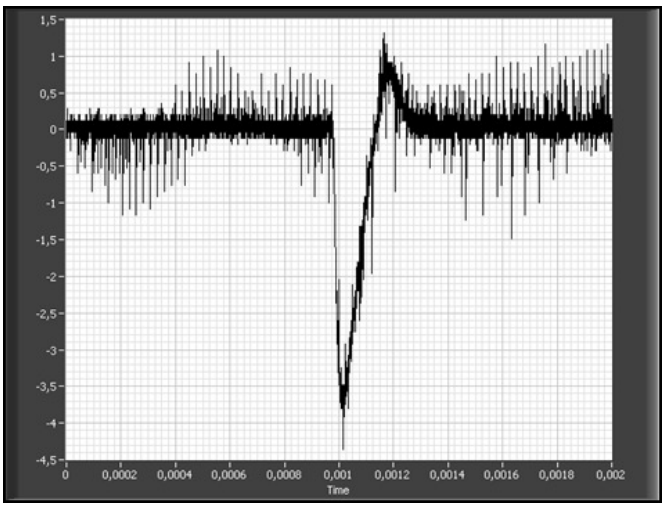

Fig. 9. Step response of a digital current converter. 2 A to 12 A load step is performed with 70 V input voltage.

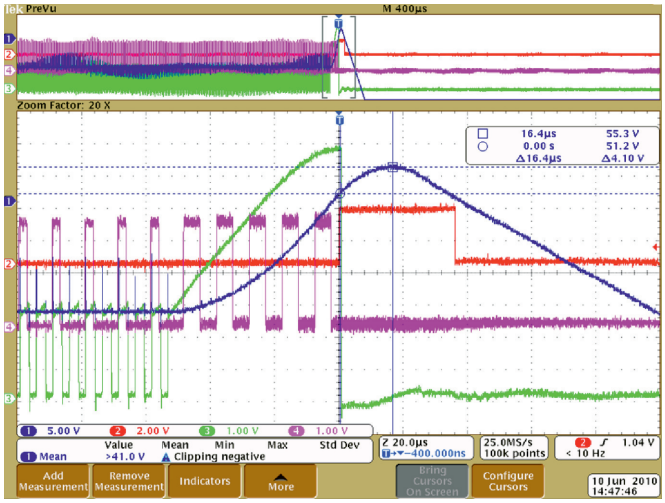

Fig. 10. Example of a pure digital overvoltage protection.

condition very fast (channel 2 goes high). The main transistor is switched off immediately (channel 3 – the current falls to zero). The output voltage (channel 1) still goes up – by more than 4V in this example. The overshoot of the voltage strongly depends on the load. Overvoltage protection based only on the main switch is not safe enough for the DC-DC converters. Additional "crowbar" circuitry to make fast short-circuit ordered by digital controller would make it possible to implement good overvoltage protection.

Characteristic feature of digital voltage frequency response plots is compressed gain at low frequencies (see Fig. 11). In theory gain falls 20 dB/decade. In case of digital voltage control, the gain roll-off is lower (it can be even flat). This depends on the number of bits in the analog-to-digital converter word. The larger the number of bits, the roll-off is closer to the theoretic value. Increasing number of bits in ADC introduces large noise in the system and causes increased jitter in duty cycle. Smaller number of bits in ADC removes the jitter by preventing the noise to enter the system at the cost of low frequency gain magnitude. The best trade off has been chosen experimentally to use 10 bits word from ADC, and all the measurements were made using this setting.

VII. Conclusion

The main objective of the task was to develop digital implementation of current mode control for medium power DC/DC converter. The main objective was met and appropriate measurements of supplied analog converter and developed digital converter were made. Concluding, it is possible to develop full functional digital current mode controller for medium power DC/DC converter.

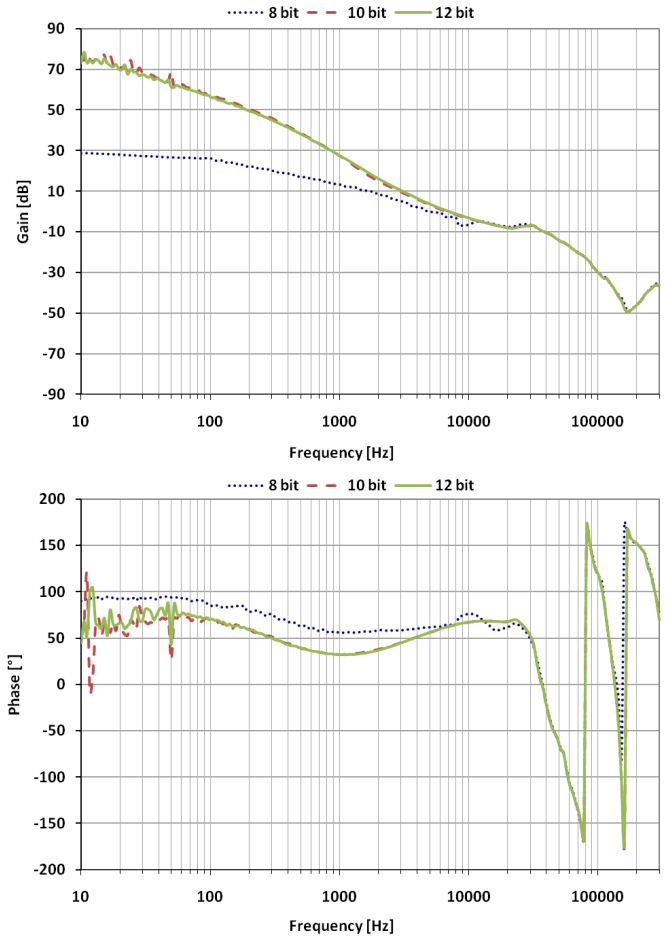

Fig. 11. Effects of ADC quantization and resolution changes in digital current mode converter.

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