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## *IMPORTANT MESSAGE FOR THE AUTHORS*

The Editorial Board during their meeting on the 18th of January 2006 authorized the Editorial Office to introduce the following changes:

1. **PUBLISHING THE ARTICLES IN ENGLISH LANGUAGE ONLY**

Starting from No 1'2007 of E&T Quarterly, all the articles will be published in English only.

Each article prepared in English must be supplemented with a thorough summary in Polish (e.g. 2 pages), including the essential formulas, tables, diagrams etc. The Polish summary must be written on a separate page. The articles will be reviewed and their English correctness will be verified.

2. **COVERING THE PUBLISHING EXPENSES BY AUTHORS**

Starting from No'2007 of E&T Quarterly, a principle of publishing articles against payment is introduced, assuming non-profit making editorial office. According to the principle the authors or institutions employing them, will have to cover the expenses in amount of 760 PLN for each publishing sheet. The above amount will be used to supplement the limited financial means received from PAS for publishing; particularly to increase the capacity of next E&T Quaterly volumes and verify the English correctness of articles. It is neccessary to increase the capacity of E&T Quarterly volumes due to growing number of received articles, which delays their publishing.

In case of authors written request to accelerate the publishing of an article, the fee will amount to 1500 PLN for each publishing sheet.

In justifiable cases presented in writing, the editorial staff may decide to relieve authors from basic payment, either partially or fully. The payment must be made by bank transfer into account of Warsaw Science Publishers The account number: Bank Zachodni WBK S.A. Warszawa Nr 94 1090 1883 0000 0001 0588 2816 with additional note: "For Electronics and Telecommunications Quarterly".

Editors

# Dear Authors,

Electronics and Telecommunications Quarterly continues tradition of the "Rozprawy Elektrotechniczne" quarterly established 54 years ago.

The E&T Quarterly is a periodical of Electronics and Telecommunications Committee of Polish Academy of Science. It is published by Warsaw Science Publishers of PAS. The Quarterly is a scientific periodical where articles presenting the results of original, theoretical, experimental and reviewed works are published. They consider widely recognised aspects of modern electronics, telecommunications, microelectronics, optoelectronics, radioelectronics and medical electronics.

The authors are outstanding scientists, well-known experienced specialists as well as young researchers — mainly candidates for a doctor's degree.

The articles present original approaches to problems, interesting research results, critical estimation of theories and methods, discuss current state or progress in a given branch of technology and describe development prospects. The manner of writing mathematical parts of articles complies with IEC (International Electronics Commision) and ISO (International Organization of Standardization) standards.

All the articles published in E&T Quarterly are reviewed by known, domestic specialists which ensures that the publications are recognized as author's scientific output. The publishing of research work results completed within the framework *of Ministry of Science and Higher Education* GRANTs meets one of the requirements for those works.

The periodical is distributed among all those who deal with electronics and telecommunications in national scientific centres, as well as in numeral foreign institutions. Moreover it is subscribed by many specialists and libraries.

Each author is entitled to free of charge 20 copies of article, which allows for easier distribution to persons and institutions domestic and abroad, individually chosen by the author. The fact that the articles are published in English makes the quarterly even more accessible.

The articles received are published within half a year if the cooperation between author and the editorial staff is efficient. Instructions for authors concerning the form of publications are included in every volume of the quarterly; they may also be obtained in editorial office.

The articles may be submitted to the editorial office personally or by post; the editorial office address is shown on editorial page in each volume.

Editors

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# Amplitude comparator for self-calibration circuit of IR mixer

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This paper presents a new sequential amplitude comparator of two sinusoidal signals. It was designed for calibration circuit of phase shifters leading to better suppression of image component in the signal path of 2.4 GHz receiver. The experimentally obtained values of IRR above 45dB after calibration process indicate that image signal rejection is very good. It enables to conclude that the conception and design of amplitude comparator is suitable. The design was performed using SiGe 0,35μm BiCMOS process.

*Keywords:* Amplitude comparator, Self-calibration of IR mixer, Image rejection

## 1. INTRODUCTION

In wireless RF receivers with low IF (Intermediate Frequency) $f_{IF}$, suppression of image signals to acceptable level is difficult. It can not be done by application of high frequency filters due to small interval between useful and image frequencies, equal to $2 \cdot f_{IF} \sim$ few MHz. Therefore special mixers are designed e.g. Hartley configuration, which eliminate (not totally of course) image signal by summing up the components of opposite phases and identical amplitudes. However effectiveness of this method depends strongly on process variations and amplitude / phase errors of heterodyne I/Q components. Hence to improve Image Rejection Ratio (IRR) an initial circuit calibration should be performed. It may be lead out [1] that

$$IRR \cong \frac{\left(\frac{\Delta V}{V}\right)^2 + \Delta\theta^2}{4},$$

where $\frac{\Delta V}{V}$ is the relative amplitude error and $\Delta\theta$ is phase error of I, Q components. Therefore the calibration process has to include two steps: amplitude balancing and phase correction.

In RF circuits a calibration process is implemented to assure stability of circuit parameters on process and temperature variations also. The calibration circuit is the integral part of receiver circuit. Usually a special RC calibration circuit with an external reference [2, 3] is applied. Sometimes a special calibration feedback loop is used [4] and [5].

In the last paper the new, effective and simple method of self-calibration applied to the Hartley architecture mixer was presented. The circuit that implements this concept contains the amplitude comparator which indicates the relation between I and Q amplitudes of image signals and shows the tuning direction of phase shifters (Fig.1). The self-calibration process is driven by digital control circuit that produces appropriate control signals for tuning the capacitance arrays in phase shifters (LPF and HPF) depending on results of amplitude comparison and phase identification processes. The method was applied in the test chip that was designed for AMS BiCMOS 0,35μm SiGe process and prototyped via Europractice. The measurements show that the value of IRR was increased by ~20dB, to above 45dB which confirms the validity of this self-calibration method and also presented in this paper new concept of amplitude comparator.

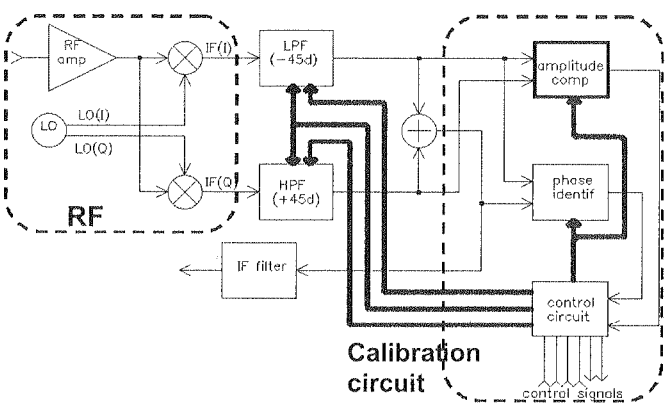



Fig. 1. Self-calibration circuit architecture

The first section describes the elaborated self-calibration method, the second section describes operation of amplitude comparator, its subsections present simulation and experimental results and the last one conclusions.

## 2. SELF-CALIBRATION METHOD

In Hartley architecture of an image-reject receiver a local oscillator with sine and cosine outputs and phase shifters ± 45° is used to obtain good image rejection (Fig.2). In theory the $u_1$ and $u_2$ components of the useful signal have identical amplitudes and phases while the image components which have reverse phases are rejected from the output spectrum after addition ($u_\Sigma$). The main drawback of this circuit is strong impact of mismatches on IRR. Process variations and parasitics existing in real circuits result in amplitude and phase errors at the adder inputs which leads to non-zero image signal on the output. In practice for integrated mixers IRR is limited to 20 dB and increasing its value is necessary.

Let's consider the circuit from Fig.2. Assuming the image components on the adder inputs:

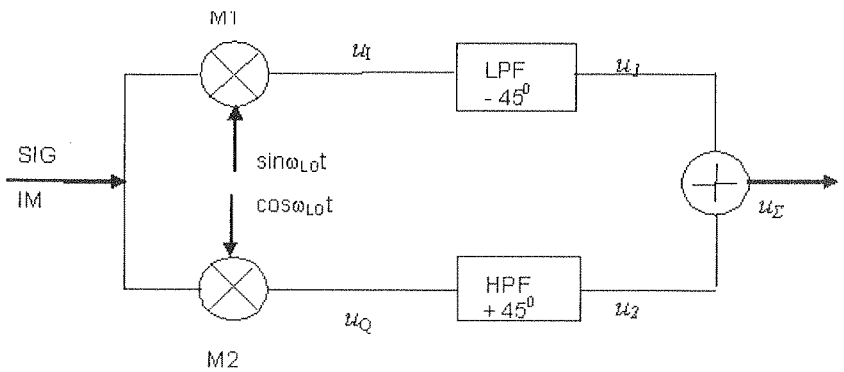



Fig. 2. Hartley architecture of IR mixer, where SIG and IM are the input signal and its image respectively, $\omega_{LO}$ is the pulsation of local oscillator signal

$$u_{1IM}(t) = U_{1IM}\sin\omega t \qquad and \tag{1}$$

$$u_{2IM}(t) = U_{2IM}\sin(\omega t + 180^0 + \Delta\Phi) \tag{2}$$

where $\Delta\Phi$ is the phase error, we have on the adder output, approximately:

$$u_{\Sigma IM}(t) = (U_{1IM} - U_{2IM})\sin\omega t - U_{1IM}\Delta\Phi\cos\omega t. \tag{3}$$

Therefore to obtain high rejection of the image signal the equalization of the adder input amplitudes and compensation or minimisation of the phase error are necessary.

In practice the -45° and +45° phase shifters are realized as one-pole low-pass (LPF) / high-pass (HPF) filters whose magnitudes and phases of the transfer functions (in the ideal case) are as follows:

$$|A_{LPF}| = \frac{1}{\sqrt{1+\left(\frac{\omega}{\omega_{pL}}\right)^2}}, \quad |A_{HPF}| = \frac{\frac{\omega}{\omega_{pH}}}{\sqrt{1+\left(\frac{\omega}{\omega_{pH}}\right)^2}}, \tag{4}$$

$$\Phi_{LPF} = arctg\left(\frac{\omega}{\omega_{pL}}\right), \quad \Phi_{HPF} = \frac{\pi}{2} - arctg\left(\frac{\omega}{\omega_{pH}}\right), \tag{5}$$

where $\omega_{pL}$ and $\omega_{pH}$ denote pulsations of the filter poles. Hence dependence (3) takes the form:

$$u_{\Sigma IM}(t) = (U_I|A_{LPF}| - U_Q|A_{HPF}|)\sin\omega t - U_I|A_{LPF}|(\Delta\Phi + arctg\frac{\omega}{\omega_{pL}} - arctg\frac{\omega}{\omega_{pH}})\cos\omega t \tag{6}$$

In the ideal circuit the produced relative phase shift is equal to 90° independently on the input frequency but the equality of $U_{1IM}$ and $U_{2IM}$ is achieved only for $\omega_{pL} = \omega_{pH} = \omega_{IF}$ and $U_I = U_Q$. The process variations of R and C values that determine the time constants in the phase shifters cause that $|A_{LPF}(\omega_{IF})| \neq |A_{HPF}(\omega_{IF})|$ which leads to inequality of amplitudes $U_{1IM}$ and $U_{2IM}$. Moreover, the amplitude error of the local oscillator quadrature signals $U_I \neq U_Q$ may occur. In this case in order to obtain amplitude balance the following equation has to be fulfilled:

$$|A_{LPF}(\omega_{IF})|U_I = |A_{HPF}(\omega_{IF})|U_Q,$$

which will be valid for $\omega_p = \omega_{pL} = \omega_{pH} = \omega_{IF}\frac{U_Q}{U_I}$.

The relative phase shift between $U_{1/m}$ and $U_{2/m}$ may be compensated by creating the following corrective phase shift:

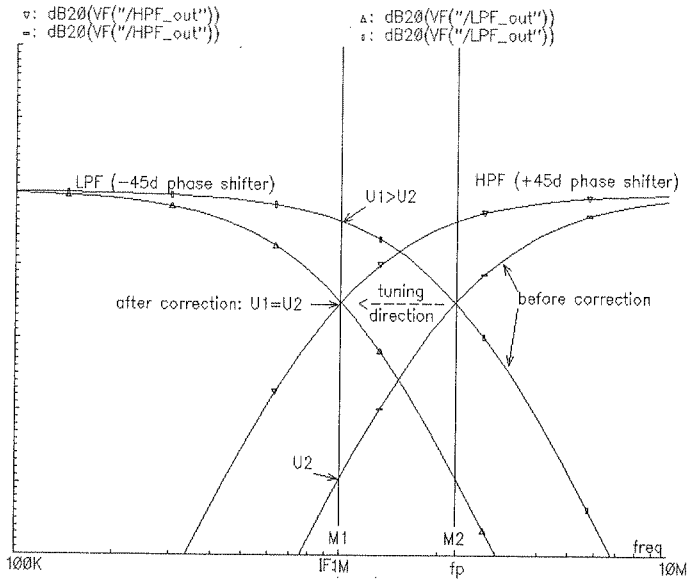
$$\Delta\Phi_{COR} = arctg\frac{\omega}{\omega_{pL}} - arctg\frac{\omega}{\omega_{pH}} = -\Delta\Phi \tag{7}$$

This will be achieved by moving the poles in the opposite directions from $\omega_p$ by $\pm\Delta\omega = \pm\frac{1}{2}\omega_{IF}tg\Delta\Phi$ (sign + for $\omega_{pL}$ and sign − for $\omega_{pH}$ when $\Delta\Phi$ is small). The moving of poles does not change the amplitude balance when $U_I = U_Q$. For $U_I = U_Q$ a small correction of the amplitude balance may be necessary.

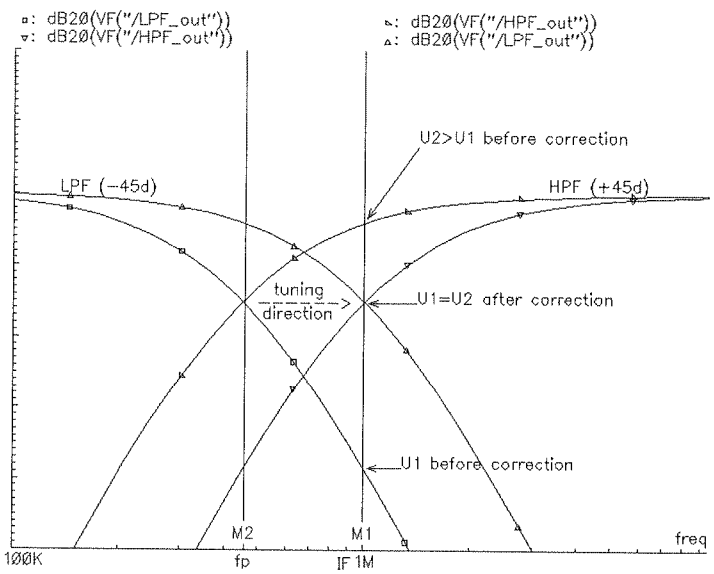
It is clear from the above that the task of self-calibration process is to minimize the amplitude difference and phase error on the adder inputs. This can be achieved by proper shifting of the poles to get equal amplitudes and generate the phase correction $\Delta\Phi_{COR}$. It is realized by the tuning filters, which play role of phase shifters in I and Q mixer paths. Therefore the calibration process has to include two steps: amplitude balancing and phase correction.

During the first step, the relation between amplitudes $U_1$ and $U_2$ determines the tuning direction of both shifters: for $U_1 < U_2$ we have $f_p > f_{IF}$ ($f_p$ – pole frequency) and the

pole frequency of each phase shifter has to be decreased (Fig.3a) until the amplitude balance will be achieved, otherwise both pole frequencies have to be increased (Fig.3b)




a) $U_{1IM} < U_{2IM}$




b) $U_{1IM} > U_{2IM}$

Fig. 3. The tuning of phase shifters during amplitude balancing

Similarly, during the second step the directions of the filter tuning are determined by comparing the phase relation between the $u_1$ and $u_\Sigma$ signals. After achieving the amplitude balance we may assume $U_{1IM} = U_{2IM} = U$, therefore according to (3)

$$u_{\Sigma IM}(t) = -U \mid A_{HPF} \mid \Delta\Phi\cos\omega t, \tag{8}$$

which gives: $u_{\Sigma IM} \div \cos\omega t$, for $\Delta\Phi < 0$, and $u_{\Sigma IM} \div -\cos\omega t$, for $\Delta\Phi > 0$, while $u_1(t) = U_{1IM}\sin\omega t$.

The adder output signal $u_{\Sigma IM}$ is shifted ±90° to its input $u_1$. The recognition of this phase makes the correct tuning of shifters possible until the change of $u_{\Sigma IM}$ phase will be noticed. This event stops the phase correction step. Fig.4 illustrates the idea of the phase error correction by tuning both shifters in opposite directions.

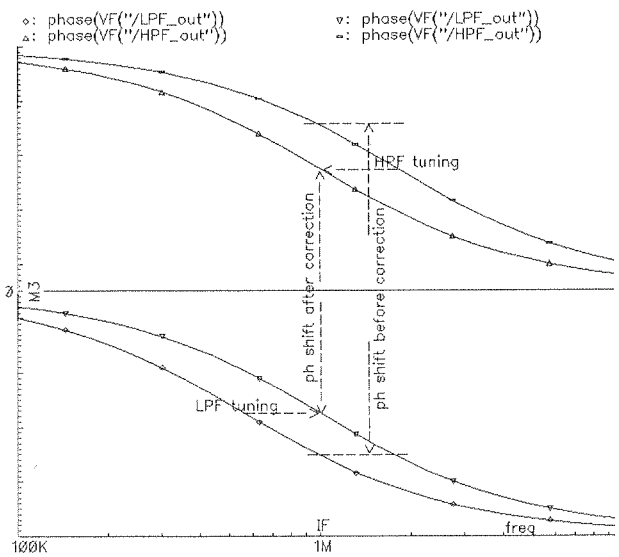



Fig. 4. The idea of relative phase shift correction

In the case of $\Delta\Phi > 0$ the pole frequency of + 45° shifter (HPF) has to be decreased and the pole frequency of – 45° shifter (LPF) has to be increased. In the opposite case the change of tuning directions of the phase shifters is required.

A convenient method of phase shifter tuning is digital control of capacitances creating its time constants. However, it introduces an unavoidable error associated with the LSB step. Let's consider the maximum value of the errors for amplitude and phase correction due to the smallest capacitance change $\Delta C$. In the vicinity of the pole the change of output amplitude due to $\Delta C$ is expressed as follows:

$$\Delta U_1 = U_I \cdot \frac{d|A_{LPF}|}{dC}\Big|_{\omega=\omega_p} \cdot \Delta C = -\pi U_1 f_{IF} R \Delta C, \tag{9}$$

$$\Delta U_2 = U_Q \cdot \frac{d|A_{HPF}|}{dC}\Big|_{\omega=\omega_p} \cdot \Delta C = \pi U_2 f_{IF} R \Delta C. \tag{10}$$

Since both shifters are tuned simultaneously and the amplitude balance will be identified by the change of relation between $U_1$ and $U_2$, the maximum relative error of amplitude balance on the adder inputs is described as follows:

$$\frac{\Delta U}{U} = \left|\frac{\Delta U_1}{U_1}\right| + \left|\frac{\Delta U_2}{U_2}\right| = 2\pi f_{IF} R \Delta C, \tag{11}$$

where other possible sources of errors are neglected.

Similarly, for the phase changes caused by the phase shifters LPF and HPF when the capacitance value is changed by $\Delta C$ we have respectively:

$$\Delta\Phi_{LPF} = \Delta C \cdot \frac{d\Phi_{LPF}}{dC}\Big|_{\omega=\omega_p}, \qquad \Delta\Phi_{HPF} = \Delta C \cdot \frac{d\Phi_{HPF}}{dC}\Big|_{\omega=\omega_p} \tag{12}$$

Taking into considerations that the tuning during the phase correction is carried in the opposite directions, the full phase change due to $\Delta C$ step is $\Delta\Phi_c = 2\pi f_{IF} R \Delta C$.

Assuming IF frequency $f_{IF}$ = 1MHz, R = 8.8kΩ, ΔU/U = 1%, $\Delta\Phi = 0,5°$ we obtain the maximum LSB capacitances $\Delta C_1$ = 180fF for amplitude balancing and $\Delta C_2$ = 160 fF for phase correction. It should provide IRR not worse than 45dB after the calibration process.

The application of the calibration method described above is limited by the minimum value of the switched capacitance used in the capacitance arrays, which depends on parasitic capacitances of the switches. It also limits the IF frequency to few MHz. Increase of the number of bits results in increase of capacitance arrays which leads to the increase of integrated circuit area.

## 3. AMPLITUDE COMPARATOR

The task of the amplitude comparator is to establish the relation between amplitudes of I, Q components on adder inputs (Fig.1) and to generate information which of them is greater. The concept of the comparison of two amplitudes of IF (1 MHz) sinusoidal waves relies on rectifying, storing and providing the DC voltages to the inputs of comparator with offset cancellation (Fig.5a). The circuit is controlled by the five-phases clock, which is generated by digital control circuit presented in [5]. The relations between phases are shown in Fig.5b.

In the circuit only one two-half rectifier is used. It is sequentially switched between two sinusoidal voltages V1, V2 and two identical storage capacitors C0, C1 (Fig.5a). Such solution allows avoiding an error caused by two different offset voltages of two amplifiers and rectifiers.

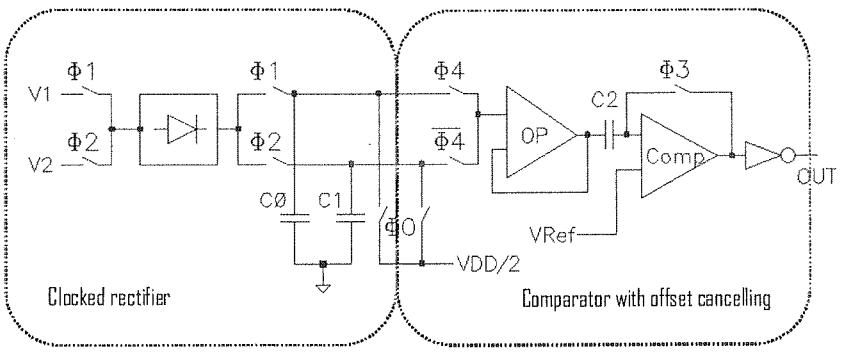



Fig. 5a. Simplified diagram of amplitude comparator

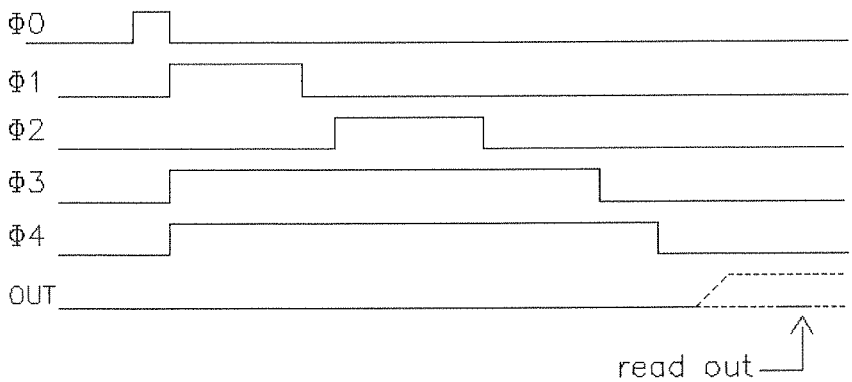



Fig. 5b. Phases Φ0 – Φ 4 used to control comparator work

Input voltages V1 = A1 - A2 and V2 = B1 - B2 (Fig.6) are attached to the inputs of differential amplifier via two pairs of switches controlled by phases Φ1, Φ2. Each of them closes the switches for 5 IF periods (5μs).

The third pair of switches controlled by $\Phi = \overline{\Phi 1 + \Phi 2}$ delivers to the differential amplifier DC voltages (D1, D2) identical with DC components of input sinusoidal voltages. Such solution allows avoiding a substantial recharging of input serial capacitors (Fig.6) and therefore eliminates the source of additional errors. The output of the differential pair is connected to the two-half transistor rectifier that is supplied with current source 15 nA. Its output (RECT), via identical switches, at phases Φ1 and Φ2, is sequentially connected to the identical capacitors C0 and C1 (7 pF). They keep the values of DC voltages for the comparation time. After comparison cycle is finished these capacitors are discharged to the VDD/2.

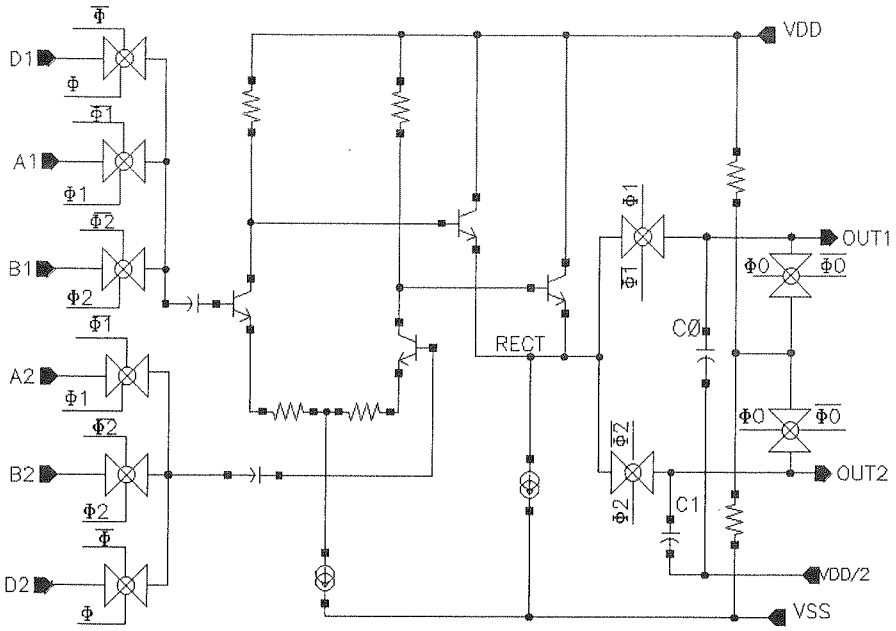



Fig. 6. Differential clocked recitifier

Next the voltages stored on C0 and C1 are delivered to the comparison circuit via the operational amplifier OPA in the follower configuration. The follower prevents discharging of C0 and C1 when they are connecxted to the capacitor C2 = 10 pF (Fig.7), what would introduce the additional error.

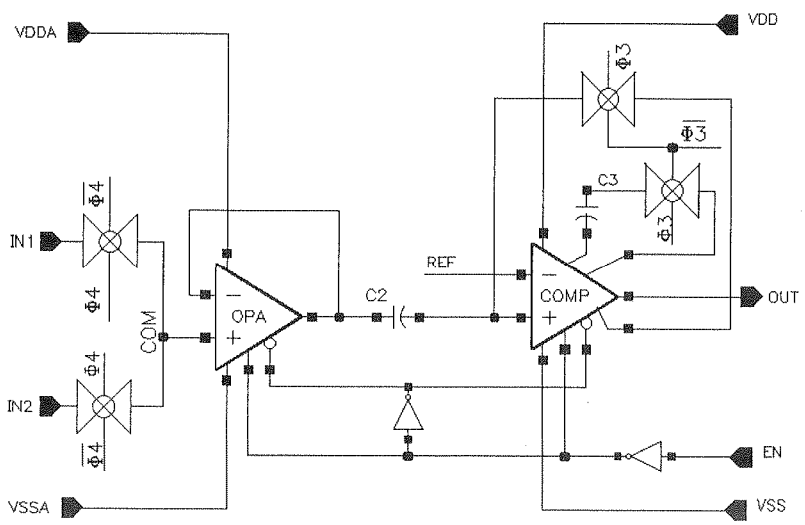



Fig. 7. Comparator with offset cancellation

The comparator COMP is a typical 3-stages one: the first stage is differential; the second stage contains frequency compensation circuit, which is connected during phase Φ3 to avoid circuit oscillation while the feedback loop is closed. The third stage has push-pull configuration.
During phase Φ3 capacitor C2 is charged to:

$$V_{C2} = V_{C0} + V_{offOP} - (V_{REF} + V_{offCOMP}), \text{ where}$$

$V_{offOP}$, $V_{offCOMP}$ are the offset voltages of opamp and comparator respectively. After switching the comparator input from $V_{C0}$ to $V_{C1}$ the comparator negative input voltage will take the value:

$$V = V_{C1} + V_{offOP} - V_{C2} = V_{C1} - V_{C0} + V_{REF} + V_{offCOMP}.$$

Then the comparator differential input voltage will be as follows:

$$V_{inCOMP} = V_{REF} + V_{offCOMP} - V = V_{C1} - V_{C0}$$

It clearly shows that reference voltage $V_{REF}$ and offsets of opamp and comparator do not influence the comparation result, assuming they are constant during comparison cycle. The possible errors may result from charge injection effect during the switches opening.

### 3.1. SIMULATION RESULTS

The amplitude comparator was simulated with *spectre* using foundry models of all devices. Fig.8 presents voltages at selected nodes to detailed illustration of circuit operation: differential sinusoidal input voltages are rectified giving VRECT that sequentially charges capacitors C0, C1 and produces VOUT1 and VOUT2 voltages at the rectifier outputs. Next, voltage on comparator input buffer VCOM and comparator output VOUT are shown. The last voltage is read out by the digital control circuit at the end of each measurement cycle and is used at amplitude balancing process.

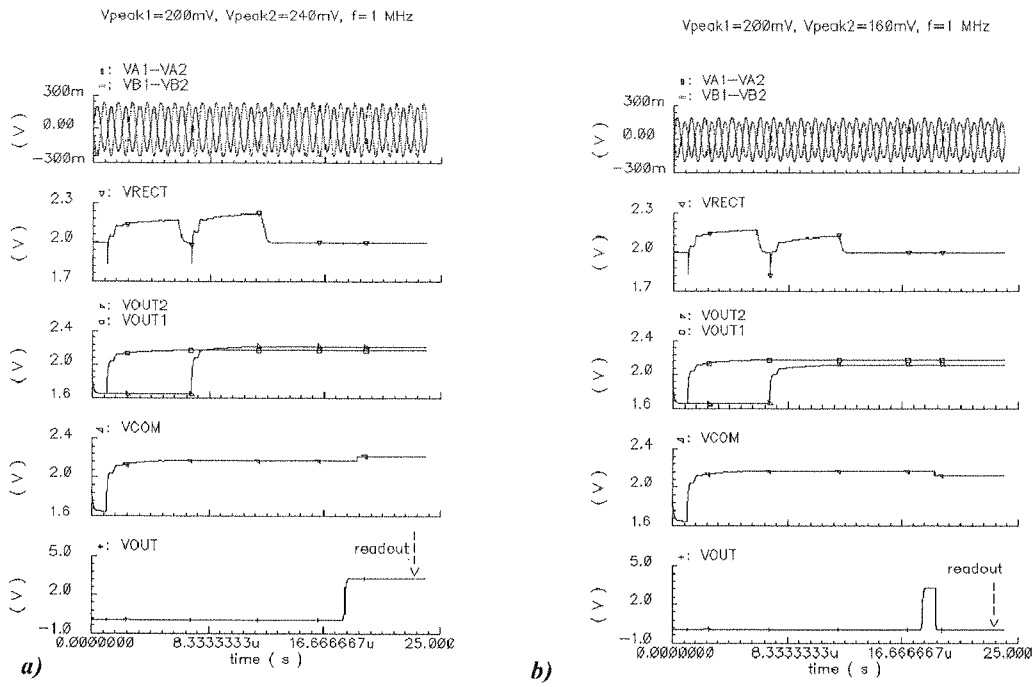



Fig. 8. Simulation results – amplitudes of compared signals ($f$ = 1 MHz) 200 mV and a) 240 mV – output state OUT = 1; b) 160mV – output state OUT = 0

Accuracy of comparation is very important because it determines the ability of image signal suppression. Therefore dependence of resolution of compared input signal amplitudes on value of the input amplitude was simulated (Fig.9).

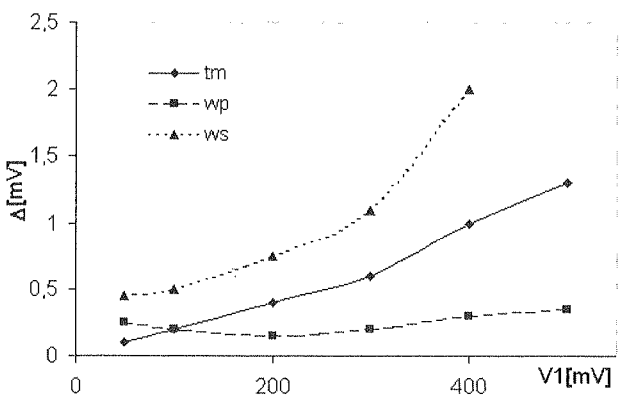



Fig. 9. Dependence of the resolution Δ of amplitude differences on value of this amplitude. Corner analysis

For amplitude values expected in the system up to ~ 200mV, the minimum resolution is better than 0,5mV. For amplitude equal 50mV the resolution $\Delta$ = 0,1mV and is greater for greater signal amplitudes. The relative resolution $\delta$ defined as the ratio of resolution $\Delta$ / amplitude [%], is independent on amplitude until 300mV (Fig.10). But even for the worst corner parameters the resolution is quite enough to use the presented amplitude comparator for balancing the amplitude of I, Q signals delivered to adder in receiver signal paths.

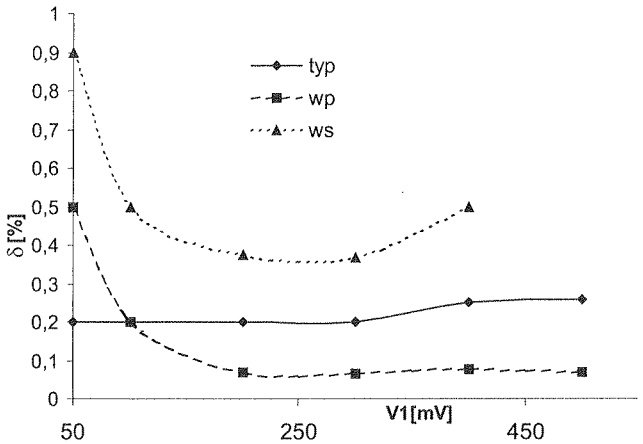



Fig. 10. Relative resolution $\delta$ of input amplitude differences. Corner analysis

### 3.2. EXPERIMENTAL RESULTS

The main goal of the measurements was to check the validity of self-calibration method of mixer with low IF = 1 MHz. The test chip was equipped with some test pins to IF path but the direct measurements of amplitude comparator were not predicted. It was planed to investigate the full calibration algorithm and the amplitude and phase calibrations separately also. Therefore full information concerning the amplitude calibration process was available.

The measurements were performed using two sets of sinusoidal 1 MHz input signals: I(0°), Q(-90°) and I(0°), Q(+90°) with various amplitudes enforced on I/Q paths of IF circuit. These signals were generated in external auxiliary circuit that allow to adjust amplitudes and phases. The measurements set up with application board were described in [5].

First the IRR without and with activated amplitude calibration for zero phase error as a function of starting amplitude imbalance (ratio of I and Q component) were measured. The results (Fig.11) confirm proper operation of the amplitude self-calibration algorithm because it increases the suppression of the image signal substantially: IRR is increased even by 35dB in the case of great initial imbalance and reaches 48dB.

The best results of IRR after amplitude calibration were obtained for initial I/Q amplitude ratio in the range 95 – 125 %.

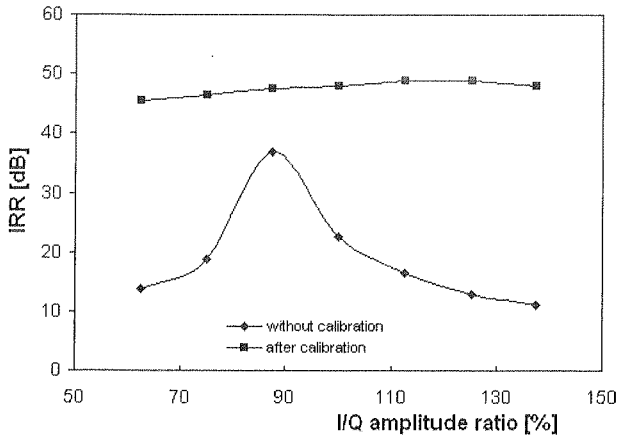



Fig. 11. Measured IRR when only amplitude calibration was performed in the case of phase error=0

Next it was interesting to measure how the calibration of amplitude affects IRR dependence on value of input voltage amplitudes (Fig.12). The best result was obtained for I/Q amplitudes in the range 60 – 80 mV.

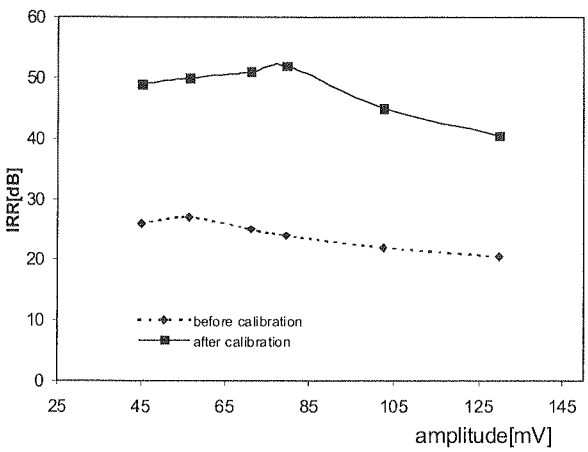



Fig. 12. Changes of IRR versus input amplitudes of calibrated signal. Phase error = 0. Only amplitude calibration was executed

The measurements indicate that the amplitude calibration process goes worse in the case of small and big magnitudes. It is nearly obvious because for small signals the absolute values of possible errors play more important role. In the case of great amplitudes a generation of harmonics of basic 1 MHz may cause an additional error.

The measurement results of IRR, performed before and after calibration process, proved the conception and the realization of the amplitude comparator presented in this paper.

## 4. CONCLUSIONS

The presented amplitude comparator was applied in the self-calibration circuit of IR mixer. It applies sequential rectifying, storing and comparison of input signals which allow to eliminate differences, which may be introduced by two separate circuits for two compared signals.
The simulations results indicate very good comparison accuracy of I and Q image components, better than $\delta$=0,2% for typical parameters.
The amplitude comparator was applied in the self-calibration circuit of IR mixer. The test chip measurements provided IRR better than 20dB in comparison to IRR before calibration and reach the value of 48dB. It confirmed the validity of the concept and the design of the presented amplitude comparator.

## 5. ACKNOWLEGMENTS

The Polish Committee of Scientific Research under Grant nr 4 T11B 03825 supported this work.

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# Performence of multichannel FX chip with DC coupled Schottky CdTe detector

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This paper describes the performance of multichannel ASIC (called FX) which has been connected to Schottky CdTe detector by DC coupling. Because of DC coupling, leakage current of the detector flows into readout electronics and changes its performance. The I-V characteristic of CdTe Schottky detector with guard ring have been measured and we have performed both simulation and experimental verification of FX IC behavior vs. detector leakage current. Due to the low values of this detector leakage current (140 pA for bias voltage of 700 V) performance of FX IC is slightly influenced. Measurements performed with low values of detector's leakage current (below 1 nA), show that the gain of readout channel stays constant with changes of leakage current, while the offset voltage at the discrimonator input changes linearly of about 4.5 mV per 100 pA of the detector leakage current. Limitations of DC coupling method are shown based on measurements with Schottky CdTe detector without guard ring, which produces higer leakage current.

*Keywords:* CdTe detector, Schottky, CdTe, DC coupled, Multichannel ASIC, CSA, PZC

## 1. INTRODUCTION

Cadmium Telluride (CdTe) detectors are very attractive for X-ray medical applications because of their large bandgap energy that allows us to operate detector at room temperature. Their high atomic numbers ($Z_{Cd} = 48$, $Z_{Te} = 52$) lead to high absorption for high energy X-ray [1]. In recent years pixel CdTe detectors have been widely used, especially in medical imaging applications [2]. To read signals from pixel detector, multichannel readout electronics are needed.

The goal of the reported research was to test the performance of multichannel ASIC chip – FX24 for operation with DC coupled CdTe detector having in mind future medical applications. The FX chip was proven to work correctly with AC coupled Si strip detectors. However, in the case of CdTe DC coupled detector, the front-end electronics should sink detector leakage current and this could influence the parameters of the readout electronics.

In this work we present leakage current measurements of Schottky CdTe detector with guard ring, simulations of the performance of a single channel of the FX chip with the detector leakage currents. We also give detailed description of measurements of Schottky CdTe detector connected with the FX chip. Finally we show the limitations of DC coupling, using for this Schottky CdTe detector without guard ring.

## 2. DETECTOR TESTS

Standard CdTe detectors which are built as structures of Pt/CdTe/Pt suffer from charge loss which reduces its energy resolution. This is caused by the low mobility and short lifetime of holes ($10^{-5} - 10^{-4}$ $cm^2V^{-1}$) compared to the lifetime of electrons ($10^{-4} - 10^{-3}$ $cm^2$ $V^{-1}$) [3]. This low mobility of holes results in charge loss, which together with large detector's leakage current, affects the performance of the readout electronics and reduces energy resolution of the total system.

However, CdTe Schottky detectors have been introduced, with leakage current strongly suppressed. Schottky CdTe detector is a structure of In/CdTe/Pt where indium is used as the anode electrode and Pt as cathode electrode for p-type CdTe semiconductor. Schottky barrier is formed at the In/CdTe interface, so one can operate detector as a Schottky diode. After biasing the detector (by applying several hundred of volts), leakage current is two orders of magnitude smaller than in standard Pt/CdTe/Pt detectors. Due to low leakage current CdTe Schottky detectors can be operated at high electric fields, which allow full charge collection.

In our test we have used CdTe Schottky detector with guard ring [4] from ACRORAD Company [5]. The detector is 1 mm thick, its size is 6.1×6.1 $mm^2$, and cathode electrode has a size of 4×4 $mm^2$. To obtain its leakage current characteristics, I/V measurement has been made in configuration shown in Fig. 1.
Detector was reverse biased by connecting high voltage source from anode's side. Cathode current, as well as ring current, were measured using indirect method of current measurement, the measurements were performed at room temperature. Figure 2 presents measured I/V characteristics of leakage currents of central electrode and guard ring. As it can be seen applying guard ring to the Schottky CdTe detector, causes cathode leakage current to be in pA range (120 pA for 700 V bias), which is at least 10 times less than in standard CdTe detectors [6]. Such low value of leakage current makes this detector a good candidate for DC coupling connection.

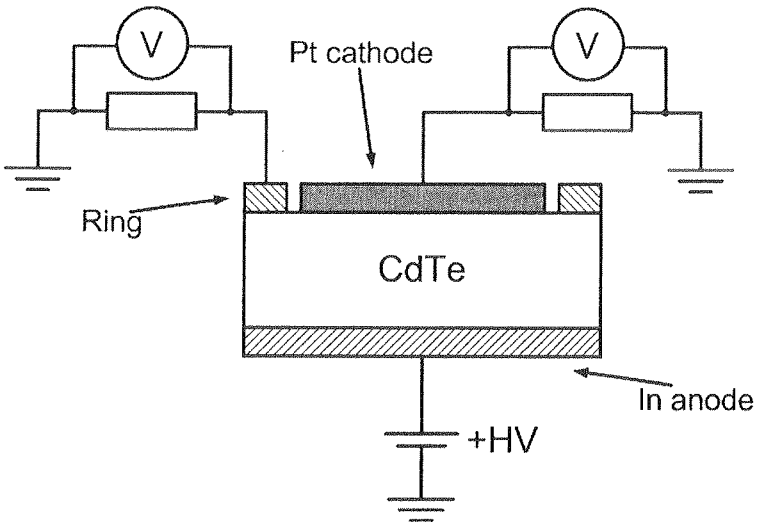


Fig. 1.

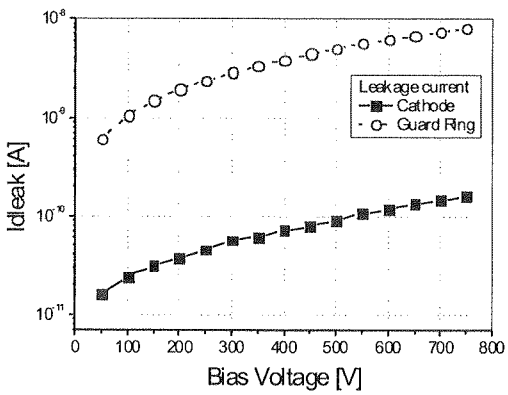


Fig. 2.

## 3. READOUT ELECTRONICS

The FX IC is a 24 channel readout ASIC designed and fabricated in CMOS 0.35 μm process [7]. Fig. 3 presents block diagram of a single readout channel of the FX chip. Each channel is built of charge amplifier (CSA) followed by pole zero cancellation circuit (PZC), a CR-RC$^2$ shaper, two discriminators and two 20 bit counters.

Charge sensitive amplifier (CSA) is based on folded cascode configuration with PMOS as an input transistor of W/L = 420 μm / 0.35 μm. Capacitance $C_f$ of 100 pF together with channel conductance of parallel connected PMOS transistors array MF0-9 working in triode region provide feedback loop for CSA. Source follower $K_1$ provides

output resistance of the CSA stage of about 0.5 kΩ. The PZC cancellation circuit consists of capacitance $C_d$ connected in parallel with fourteen PMOS transistors $M_{PZ}0$-13 operating in triode region.

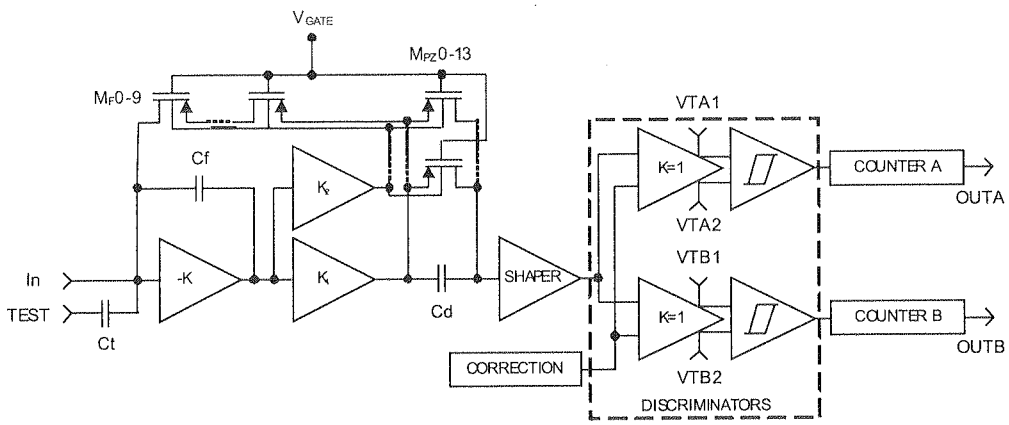


Fig. 3.

Bulks of $M_F$ and $M_{PZ}$ transistors are connected to CSA output through the source follower $K_2$, therefore the bulk voltage tracks changes of CSA output. Effective resistances of CSA feedback and PZC circuit can be controlled in a wide range (several MΩ to tens of GΩ) by the internal 5-bit DAC. Pulses after second order shaper stage with a peaking time $T_P$ = 75 ns are selected by two discriminators according to their amplitude.

Such circuit works properly even up to about 2 MHz of average rate of input pulses. The noise performance measured with AC coupled silicon strip detector ($C_{DET}$ = 1 pF) is below 150 electrons rms.

Because CSA, shaper and discriminators are DC coupled, and the common threshold level is applied to the multichannel system, a problem of the DC level spread at the discriminator inputs has been solved by the implementation of a correction DAC in each channel. Correction offset can be set up in range of 60 mV with 7 bit precision it is implemented in each channel independently. This can be helpful in operation with DC coupled strip or pixel detector where we expect the spread of the detector leakage current between the channels.

## 4. SIMULATIONS OF READOUT ELECTRONICS WITH A DC COUPLED DETECTOR

Presented circuit was simulated with the use of HSPICE software. Input of CSA was triggered with square current pulses (1 ns rise and fall time, 9 ns pulse width) with various amplitudes to simulate an injection of holes (or electrons). Voltage response at

the shaper output for positive input current signals with different amplitudes is shown in the picture below (Fig. 4). In these simulations the detector leakage current was set to zero. The gain of the front-end electronics calculated from these simulations is 50.4 μV/el.

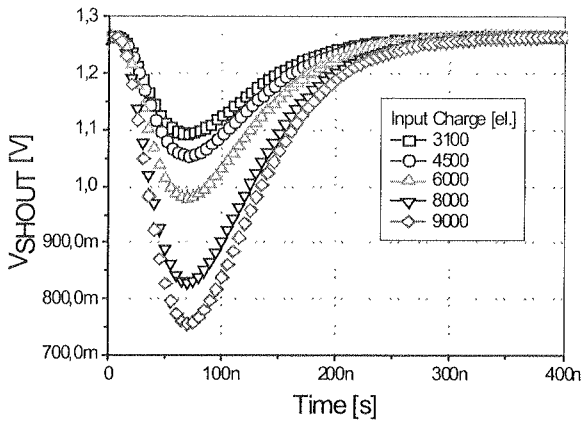


Fig. 4.

Because readout electronics is DC coupled with the detector, leakage current from the detector modifies its parameters. Simulations of leakage current influence on electronics performance were done by adding DC detector leakage current component during the HSPICE simulation. Figure 5a shows shaper output for different values of leakage current.

It can be observed that the offset voltage shifts with the increase of leakage current. In the range of leakage current 0 – 3 nA offset voltage changes by 112 mV (about 10 %) for setting the CSA feedback resistor to tens of MΩ. Also the amplitude of output signal changes but only by 2 mV (about 0.6 %), so the changes in the offset voltage are of the main importance. However, in the range 0-160 pA of presented detector leakage current (Fig. 5b) offset voltage changes only by 8 mV (about 0.6 %). As it was mentioned, a correction circuit is present in FX chip to reduce channel to channel DC level spread at the discriminator input. However, it can also be used for suppressing offset voltage caused by the spread of the detector leakage current is multichannel system.

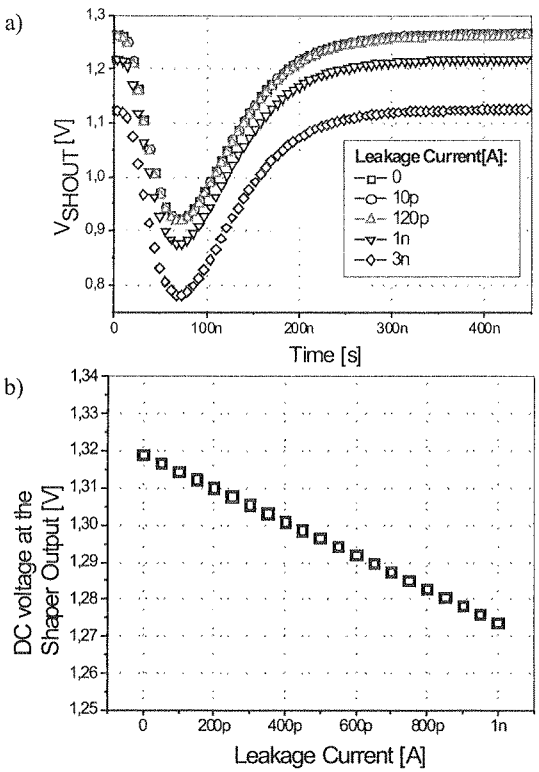


Fig. 5.

## 5. MEASUREMENTS OF SCHOTTKY CDTE DETECTOR WITH GUARD RING CONNECTED TO FX INTEGRATED CIRCUIT

Detector's cathode was connected to single channel of FX ASIC by DC coupling (Fig. 6). Guard ring of the detector was connected to ground potential. Anode electrode was supplied with high voltage. Input signals for readout electronics were generated by on-chip internal calibration circuit.

This configuration assures that leakage current of cathode electrode of the detector flows into readout electronics, therefore influence of leakage current can be measured.

Because the FX circuit has a binary architecture, the basic analogue parameters (offset, gain) can be obtained by scanning the threshold of discriminator for a given amplitude of input pulses. At the output we measure the fraction of pulses which exceed the discriminator threshold and trigger the comparator.

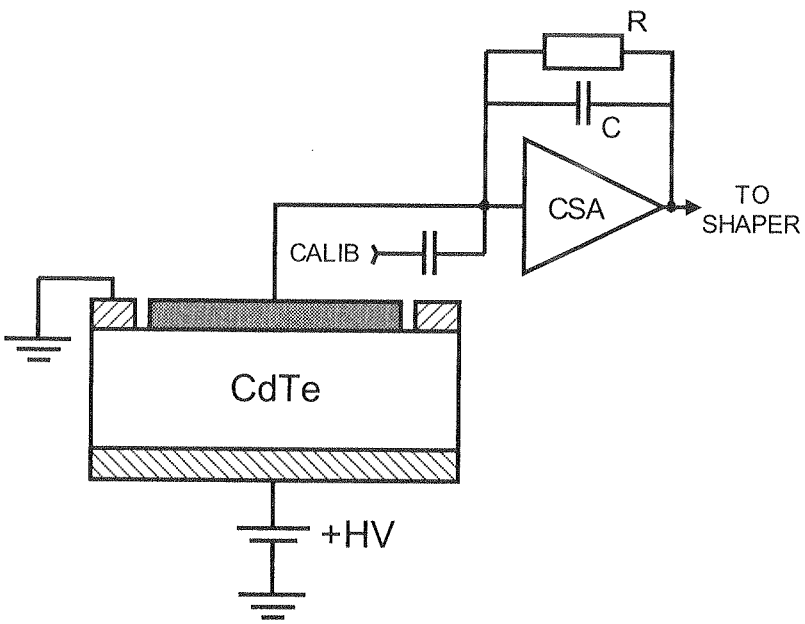


Fig. 6.

Measurements were performed for different values of leakage currents and different values of amplitudes of input signals. Making a threshold scan and differentiating the measured integral distribution we find the peak positions for different values of bias voltages.

For given amplitude of input pulses the peak position shifts as the bias voltage of the detector increases from 100 V to 700 V. The changes of the peak position are linear and for the leakage current changes from 25 pA to 140 pA peak position changes of about 6 mV (Fig. 7a). From the measurements with different amplitudes of input pulses we find the gain of our readout electronics. The gain (Fig. 7b) is constant in the range of applied detector's bias voltage. It means that the shift of peak position is caused by the DC level voltage shift at the shaper output and the measured shift of peak position is in a good agreement with earlier simulations.

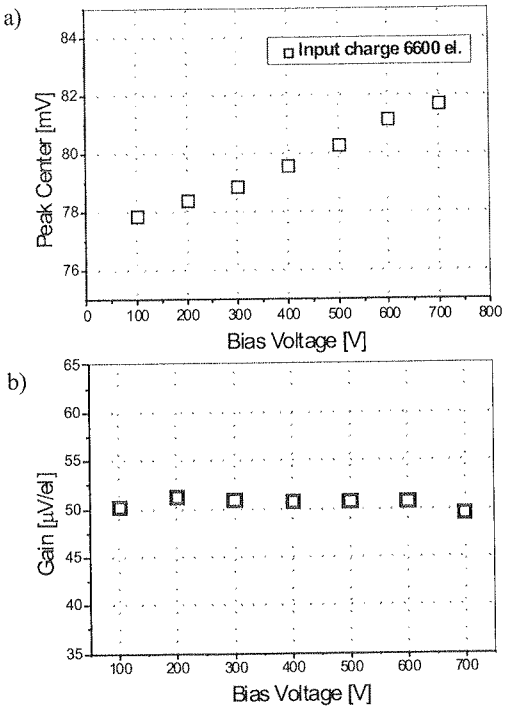


Fig. 7.

## 6. DC COUPLING TECHNIQUE LIMITATIONS DUE TO HIGH DETECTOR LEAKAGE CURRENT

For some applications DC coupling may not be suitable because of large leakage current of the detector (in range of few nA). One of the reasons of leakage current rise may be a need to use the detector without guard ring. Detectors without guard ring are needed when they are used in matrix of sensors, where guard rings would cause dead space in the detector's area, decreasing its performance.

Having in mind future applications, simulations of FX24 readout electronics and measurements with CdTe Schottky detector without guard ring were made to determine how large values of detector's leakage current influence the readout performance.

From the simulations performed it can be observed (Fig. 8) that with detector leakage current rising up to a few nA, gain of readout electronics drops (by 3 % for 2 nA , up to 60 % for 10 nA) and significant shift of offset voltage is present (from 150 mV for 2 nA up to 350 mV for 10 nA).

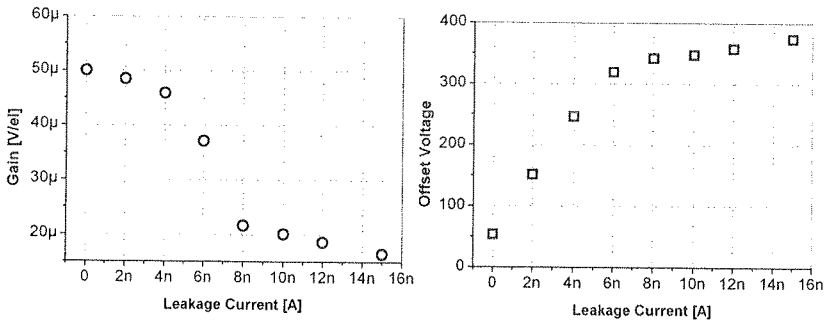


Fig. 8.

For measurements Schottky CdTe 4×4 pixel detector was used. The detector is 1 mm thick, its size is 4 × 4 $mm^2$. This detector did not have a guard ring. Firstly, five channels of the detector were DC coupled with the FX24 chip. The rest of channels were left floating.

Large shift of offset voltage (around 300mV) and gain drop (down to 30 µ V/el) was observed from X-ray measurements (X-ray beam energy – 18keV) performed with detector bias voltage equal to 200 V. Noise estimated from calibration pulses is around 200 el., noise estimated from X-ray measurement is around 250 el.

The same detector was connected to the FX chip via AC coupling (Fig. 9), using SMD capacitor (47 pF) and SMD resistor (100 MΩ). Thanks to the AC coupling large detectors leakage current does not influence the performance of readout electronics, so large values of bias voltage can be applied to increase detector's charge collection. The gain from measurements is estimated to 51 V/el., which is the same as with low leakage current DC coupled version. Noise calculated from X-ray measurements is around 146 el.

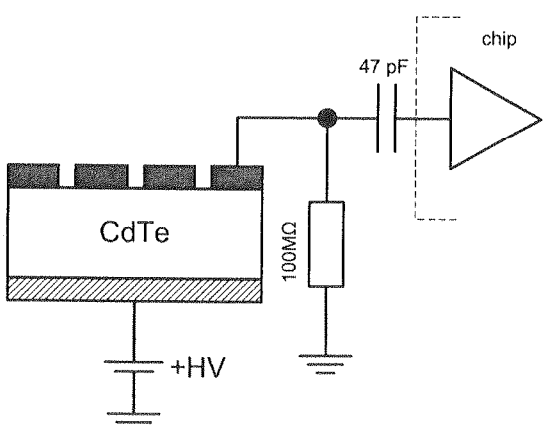


Fig. 9.

## 7. SUMMARY

The performance of the FX integrated circuit working with DC coupled CdTe Schottky detector was presented. Simulations of FX single readout channel were performed with the use of HSPICE software to determine the influence of leakage current on channel parameters. After connecting the detector to FX chip, measurements were performed. The data obtained from measurements matches with simulations confirming that low leakage current (below 1 nA) of CdTe Schottky detector, equipped with guard ring, have very little influence on FX chip parameters.

However, leakage current of few nA and more causes degradation of FX chip performance, making DC coupling not suitable for this application. As it was presented, AC coupling connection between the detector and readout chip can be used to suppress the influence of leakage current.

## 8. ACKNOWLEGMENTS

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# Asynchronous Circuits through SystemC Description

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Asynchronous design is fundamentally different and not yet a well-established methodology. An important obstacle to growth of this methodology is lack of CAD tools to design circuit automatically. The starting point in developing a circuit is its modeling and simulation. At this paper we will propose an asynchronous library as extension to SystemC language to enable asynchronous circuit description at the highest level of abstraction. For this purpose, channel, join, fork, mux, demux, and merge that are basic elements of asynchronous circuits are introduced into the library. Also a tool was developed which extracts optimized control flow graph and data flow graphs from the high level description. By using proposed library modeling and designing of efficient asynchronous circuits can be done without having to deal with detail of asynchronous implementations. Extracted CFG and DFG were prepared in well-defined form that can easily be used for synthesis purpose, verification or test generation in later steps of our digital design flow.

*Keywords:* Asynchronous Circuit, SystemC, High-Level Modeling, CFG and DFG Extraction

## 1. INTRODUCTION

As CMOS manufacturing technology scales into deep and ultra-deep sub-micron design, problems with clock skew, clock distribution, and on-chip communication in high-speed synchronous designs are becoming increasingly difficult to overcome. On the other hand, general interest for embedded and portable systems enforces the designers to think about on power metric in the design. In addition to this difficulty, design of complex System-On-Chip structures in VLSI circuits produces new challenges. At this high massive integration level synchronizing all blocks of a large SoC to a unique global clock definitely decreases the performance of digital system and the clock di-

stribution tree should expand in all over the SoC, so has a lot of overhead in wiring, area, and power in digital system.

Asynchronous circuits have potential advantages to become an option in various application areas. One of the biggest claims to fame for asynchronous logic is that it consumes less power due to the absence of a clock. Other advantages of asynchronous circuits are low latency, higher performance, and lower electromagnetic interference. However, there are some obstacles that avoid asynchronous design to become a feasible solution. One of the most important problems is the lack of appropriate CAD tools. Designers have to use synchronous tools with tricky modifications to fool them into thinking that the design is synchronous, making logic design verification, timing rollups, and race condition checks messy and involved.

Almost all of the languages for asynchronous circuit designs are based on CSP [1] that hides the details of handshaking protocols.CHP [2], Balsa [3], OCCAM [4] and Tangram [5] are other examples of asynchronous language. Most of existing languages for asynchronous system design have different structure from well-known synchronous system design language (e.g. Verilog or VHDL), so they are specific for asynchronous design and could not be used instead of synchronous language. Also their simulation tools are not completely available. In spite of traditional CSP based languages for asynchronous circuits other effort was also done previously. Hofer et al. [6] present an asynchronous SystemC library to model asynchronous circuits and especially NoCs. They introduced some style in SystemC like handshaking, channels, parallel operators and arbiter that is useful for describing NoC structures. In [7] a method for synthesizing object oriented structures in SystemC to achieve synchronous circuits was presented.

To overcome difficulty in modeling and simulating asynchronous circuits we propose an asynchronous library for SystemC [8] language. In addition to this library, a tool which extracts control-data flow structure from Asynchronous-SystemC is presented. A readable intermediate representation for this flow is proposed to accommodate the design specification with the vision of optimization capabilities in the conversion step.

Section 2 discuss on features of the SystemC in describing digital circuits, especially asynchronous circuits. Proposed library components will be illustrated in Section 3. Section 4 expresses steps involved in extracting Control Data Flow structures from Asynchronous SystemC Code. Section 5 contains related case study to demonstrate the features of our modeling strategy and the conclusion will be drawn in last section.

## 2. FEATURE OF SYSTEMC IN MODELING DIGITAL CIRCUITS

### 2.1. SYSTEMC POTENTIALITY

SystemC is a system design language based on C++ that has been developed in response to the need for a language capable of improving the overall productivity for designers of electronic systems. Strictly speaking, SystemC is not a language, but

rather a class library within a well established C++ language. Hence every feature of C++ can be used in modeling hardware. Some C++ features like object oriented and polymorphism enable the designer to use this concept in SystemC to model circuits and simulate them with available tools. Another superiority of SystemC is the Template feature and parameterized hardware description, which enables the reusability of design compared to common HDLs.

SystemC provides event objects and dynamic sensitivity to facilitate hardware modeling in behavioral model and concurrent software. Most HDLs offer static sensitivity: process respond to events on input signals and ports that are predetermined at elaborate time. In addition to the static sensitivity, SystemC offers dynamic sensitivity: processes can wait explicitly on events that are determined at run-time [9]. We use this feature to promote our asynchronous circuit modeling to synchronize hardware blocks at run-time. This higher level of abstraction gives the design team a fundamental understanding early in the design process of the intricacies and interactions of the entire system and enables better system tradeoffs, better and earlier verification, and overall productivity gains through reuse of early system models as executable specifications [10]. SystemC provides mechanisms crucial to modeling hardware while using a language environment compatible with software development. Major hardware-oriented features implemented within SystemC include: Time model, Hardware data types, Module hierarchy to manage structure and connectivity, Communications management between concurrent units of execution, Concurrency model [10].

### 2.2. WEAKNESS OF SYSTEMSC IN MODELING ASYNCHRONOUS CIRCUIT

In asynchronous design there is no global synchronization clock signal; meaning that every module operates separately and the synchronization is performed by handshaking signals. Handshake signals can be modeled by channels in SystemC, although there are some points that must be considered. Suppose that in the handshake channel, one side put data and the other side takes data when it becomes available. For modeling this transaction we need a channel that doesn't store data in a buffer (in other words it must be memory less). Also the first side must block further action until the data is taken at the other side. Native SystemC uses sc_signal or sc_fifo; however the former is non-blocking and the latter is not memory-less so they do not satisfy the requirement for modeling an asynchronous handshaking.

According to the asynchronous technique requirements, in handshaking modules some refined channels are necessary to model one-to-many and many-to-one channels; the first is to implement the fork operation and the second the join operation.

A strong point of SystemC is its simulation kernel that enables us to create events and handle synchronization. In the following section we will propose a way to solve these issues.

## 3. COMPONENT OF LIBRARY

SystemC implements a discrete time computation model. Processes are basic units of concurrent activities and are grouped into modules. Modules can contain other modules, allowing the hierarchical construction of the system model. Processes communicate with each other via interfaces, channels and ports, and can synchronize with each other via events objects. Interfaces define a set of related communication methods. An interface defines an abstract type, and does not implement any functionality. Ports are declared as being associated with a particular interface. The port's methods call the methods of the interface. Channels implement one or more interfaces. When connecting two modules together, the channel could offer one interface to one module, while offering a different interface to another.

In the asynchronous circuits an active process initiates a transaction by sending a request signal to the passive process. Active and passive processes bind to each other using channels. An active process may put data into a channel or get data from it. According to the direction of the request signal and data we categorize channels into two types: Push and Pull channels where in the first one the direction of the request signal and data is the same.

### 3.1. INTERFACES

According to the above categorization, for the process type (active or passive) and the operation on channel (write or read), we define four interfaces for asynchronous channels:

- AIF_ACT_WR: Asynchronous active write interface
- AIF_PAS_ WR: Asynchronous passive write interface
- AIF_ACT_RD: Asynchronous active pull interface
- AIF_PAS_RD: Asynchronous passive pull interface

Fig 1. shows the implementation code of AIF_ACT_WR. In Fig 1. , put provides a method to initiate the transaction, probe provides a method to verify the channel status to know if the data are taken at other side. rd_event returns an event when the pull side of the channel picks the data. write_block is a method that uses the above methods to perform a blocking write in the push channel.

```
template<class T>
class AIF_ACT_WR: virtual public sc_interface{
public:
   virtual void put(const T& data) = 0;
   virtual bool probe() = 0 ;
   virtual const sc_event& rd_event() const = 0;
   virtual void write_block(const T& data) = 0;
};
```

Fig. 1. Implementation of active write interface

### 3.2. PORTS

Ports to a module are like pins to a chip that enable communication between modules. According to the section 4.1 categorization we need four port types:

- AACT_OUT: Asynchronous active output port
- APAS_IN: Asynchronous passive input port
- AACT_IN: Asynchronous active input port
- APAS_OUT: Asynchronous passive output port

All implementations are template based increasing the reusability of the description.

### 3.3. CHANNELS

Channel between modules is like the interconnection and buses between chips. We implement two types of channel: ACH_PUSH and ACH_PULL channels. The first channel is a class that derives from AIF_ACT_WR and AIF_PAS_RD interface classes and implements their virtual methods. The pull channel derives from AIF_PAS_WR and AIF_ACT_RD interface classes. Fig 2. presents a diagram of these concepts. In Fig 2. the larger arrow shows the direction of data and the smaller arrow represents the request signal direction.

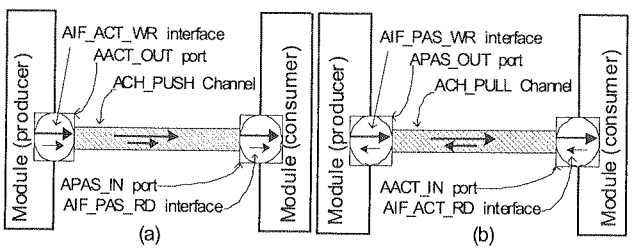


Fig. 2. Diagrams of (a) a push channel (b) a pull channel

### 3.4. SYNCHRONIZATION MODULES

In the previous subsection, we presented a method to model asynchronous synchronization between two modules. Now, we present the synchronization among more than two channels. Also we introduce the modeling methodology for building blocks of asynchronous circuits [20], which are a minimum set of components sufficient to implement asynchronous circuits that contain latches, function blocks, unconditional and conditional flow controls. The first and second are similar to synchronous circuits, so we describe the third and fourth.

### 3.4.1. UNCONDITIONAL FLOW CONTROL

Fork and join components are used to handle parallel threads of computation. Forks are used when the output from one component is input to more components; Joins are used when data from several independent channels needs to be synchronized – typically because they are (independent) inputs to a circuit. A merge component has two or more input channels and one output channel. Handshakes on the input channels are assumed to be mutually exclusive and the merge relays input tokens/handshakes to the output. For each of these components we present a class where their data type is template class, increasing their flexibility. Fig 3. presents an example of a join operation that synchronizes two input stream handshakes since their outputs are synchronized.

```
#include <systemc.h>
#include "asynch.h" // defined in our library
#include "JOIN.h"   // defined in our library
int sc_main (int argc , char *argv[])
{// Module instantiation
   producer<char> prA("RandomGen1");
   producer<int>  prB("RandomGen1");
   consumer<char>  coA("consumer1");
   consumer<int>  coB("consumer2");
// Channel instatiataon
   ACH_PUSH<char> A("ch1"),Async_b("ch2");
   ACH_PUSH<int> B("ch2"),Bsync_a("ch4");
// synchronization operation instantiation
   JOIN<char,int>     join("join1");
//Module Binding
   prA(A);
   prB(B);
   join(A, B, Async_b, Bsync_a);
   coA(Async_b);
   coB(Bsync_a);
   sc_start(-1);
   return 0;
}
```

Fig. 3. Synchronize channel A & B by Join

### 3.4.2. CONDITIONAL FLOW CONTROL

MUX and DEMUX components perform the usual functions of selecting among several inputs or steering the input to one of several outputs. These components like the unconditional flow control can be described in our library to ease asynchronous circuit modeling in SystemC. Fig 4. shows the implementation of a two-input MUX in our library for push channels. We assume that all three inputs must become available, before the output of MUX becomes active.

```
class ADD_SUB : public sc_module
{
public:
APAS_IN<sc_uint<8> > A,B;
APAS_IN<bool>    C;
AACT_OUT<sc_uint<8> > R1,R2;
SC_HAS_PROCESS(ADD_SUB);
ADD_SUB(sc_module_name name): sc_module(name)
 {    SC_THREAD(func1);   }

void func1(){
sc_uint<8> a,b,r1,r2;
bool c;
while (true) {
/*Parallel Passive read*/
  while(!(A->probe()&&B->probe()&&C->probe()))
wait(A->wr_event()|B->wr_event()|C->wr_event());
  A->get(a); B->get(b); C->get(c);
  /*Function block*/
  if(c){ r1=a+b; r2=a-b; } else { r1=a-b; r2=a+b; }
  /*Parallel Active Write*/
  R1->put(r1); R2->put(r2);
  while( R1->probe() || R2->probe())
    wait(R1->rd_event()|R2->rd_event());
}}

void func2(){
sc_uint<8> a,b,r1,r2;
bool c;
while (true) {
  PAR_PAS_READ(A, a, B, b, C, c);
  if(c){ r1=a+b; r2=a-b; } else { r1=a-b; r2=a+b; }
  PAR_ACT_WRITE( R1,r1, R2, r2);
}}};
```

Fig. 4. Implicit synchronization inside the function body

### *3.4.3. IMPLICIT FLOW CONTROL*

An inter-module synchronization was presented by using explicit modules (join, fork, etc.) in the last two subsections. A flexible way is to synchronize channel inside the modules, we call it implicit synchronization.

Fig 4. presents an example that implements an arithmetic module. There are two functions (func1 and func2) in Fig 4. with the same functionality. In the first function we use the raw capability of our library, whereas in the second one we use some macros to handle synchronization between channels. Although the first method needs more lines of code, it is more flexible than the second one. MERGE, PAR_PAS_READ, PAR_ACT_READ, PAR_PAS_WRITE and PAR_ACT_WRITE are macros that could be used to handle synchronization implicitly. The last four macros were used to read or write the variables in function body from or to channels in parallel. Parameters of MERGE macro is a series of input channels and a variable. The macro sets variables with the activated channel number. For example, in the following line sel_var is set to 0, if ch1 becomes active, or it is set to 2 if ch3 becomes active. In all cases the variable out is set to the activated channel content.

MERGE(ch1,ch2,ch3,ch4,sel_var,out);

The first four macros can be used to implement an unconditional flow control whereas the MERGE macro is used to implement a conditional flow control inside the modules.

## 4. CONTROL DATA EXTRACTION FROM ASYNCHRONOUS SYSTEMC LIBRARY

### 4.1. SYNTHESIZABLE CONSTRUCTS

The presented tool extracts control and data flow structures from SystemC 2.0.1 constructs complemented with asynchronous library described in previous section. Hierarchical description can be done by using SC_MODULE constructs in SystemC. A repeated sequential task is modeled by means of functions.

According to the asynchronous circuit properties, the communication is modeled with dynamic sensitivity; thus we employ SC_THREAD construct in SystemC to model concurrent blocks inside the module. Concurrent blocks are composed of instantiated modules and SC_THREAD blocks; these asynchronous blocks communicate with each other through asynchronous channels. Inside each concurrent block, there exist sequential constructs such as if-then-else, switch-case, for-loop and function call.

### 4.2. INTERMEDIATE REPRESENTATION

The extracted control flow determines the execution order of constructs in sequential bodies (function or sc_thread), as well as blocks dependencies in concurrent bodies (sc_module). The extracted data flow represents arithmetic and logical operations. It is composed of operational nodes and their operands edges.

#### *4.2.1. CONTROL FLOW*

Intermediate representation for control structures is composed of two types: hierarchical and sequential constructs. Fig 5. shows hierarchical constructs, MOD for module declaration, FUN for function declaration, THR for sc_thread declaration and MDI for module instantiation are used.

| | |
|---|---|
| MOD;id;chan_list<br>/*module body*/<br>DOM;<br>FUN;id;param_list<br>/*function body*/<br>NUF; | MDI;id;port_list<br>chan_list := (chan)+<br>chan := type;width;name;<br>type := PI\|PO\|AI\|AO<br>port_list := (port)+<br>port := width;name;<br>param_list:= (param)+<br>param := dir;width;name<br>dir := input\|output\|inout |
| THR;id;<br>/*thread body*/<br>RHT; | |

Fig. 5. Hierarchical control structures

'+' expresses one or more iteration, and '|' states alternation between choices. In these structures "id" is a unique number at each level of hierarchy. The "width" in above constructs presents data width of channels, ports or parameters. The "type" of channels is shown with PI (passive in), PO (passive out), AI (active in) and AO (active out).

| | |
|---|---|
| if_control;id;dfgId;dfgPortList;<br>{ if;id;dfgId;variable;<br>//sequential body<br>fi; }+ | dfgPortList:=(dfgPort)+<br>dfgPort:=dir;param<br>dir:=IN\|OUT<br>paramList:=(param)+<br>param:= variable\|constant<br>chanVarList := (chanVar)+<br>chanVar:=channel;variable |
| RETURN;id;dfgId;dfgPortList; | |
| loop;id;dfgID;dfgPortList;<br>//sequential body<br>pool; | CALL;id;funId;paramList; |
| PAR_PAS_READ;id;chanVarList;<br>PAR_ACT_READ;id;chanVarList;<br>PAR_PAS_WRITE;id;chanVarList;<br>PAR_ACT_WRITE;id;chanVarList; | CALL;id;funId;paramList; |
| | |

Fig. 6. Sequential control structures

Sequential constructs are used inside the body of FUN and THR blocks, where their order is important in data flow. Fig 6. depicts sequential control structures. In fig 6. "id" represents the order of constructs. The construct "if" is used for the implementation of if-then-else or switch-case structures, for each of these construct there is an "if_control" node and some "if" constructs. In "if_control" dfgId is the ID number of data flow graph used for evaluation of conditions and dfgPortList contains its inputs and outputs. The body of "if" is executed when "variable" evaluates to a non-zero value. All "if" constructs which are in the same group, have identical "id" numbers. "PAR_X_X" constructs represent channel operations that read channels to variables or write variables to channels. "RETURN" is used inside the function in place of "return" in SystemC, "loop" is used for iterative constructs, a DFG is used to compute the loop condition, and "VA" is used for variable assignment. In these constructs dfgId is the ID of DFG that computes an expression with its parameters in dfgPortList. "CALL" constructs are used for function calls where "funId" is the called function ID.

#### 4.2.2. DATA FLOW

The extracted data flow is shown by means of Data flow Graph (DFG) where nodes represent arithmetic or logical operations and edges show the flow of data. Each DFG has an ID that maps to a construct in the control flow.

### 4.3. IMPLEMENTATION

The flow-graph representation of the high-level description is obtained by parsing the input Asynchronous SystemC code. Fig 7. depicts the various steps involved in this methodology. These steps are quite similar to the phases of a compiler, each of which transforms the source program from one representation to another.

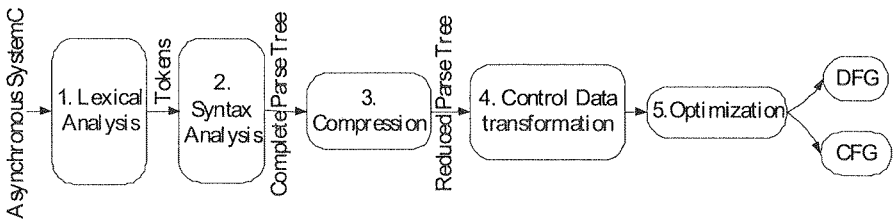


Fig. 7. Steps involved in Control Data extraction

The lexical analysis phase translates the source program into a stream of tokens, where each token is a sequence of characters with collective meaning, such as an identifier, a keyword, an operator or a punctuation character. This stream of tokens is further subjected to syntactic analysis which imposes a hierarchical structure on them to verify the syntax of the program. The codes from these two phases are generated by applying the standard compiler construction tools, Lex and Yacc.

The parsing of the tokens using YACC code imposes a hierarchical structure that could be visualized as a tree-structure (parse tree). The parse tree that is assumed to be available is just a conceptual visualization of the syntactic structure of the program. Explicit codes are required to extract such a parse tree from the YACC code. Specific C++ codes were used for this purpose in our tool. The parse tree, thus obtained, is further compressed to obtain a syntax tree in which the operators appear as the interior nodes, and the operands of an operator are the children of the node for that operator. The syntax tree is transformed, through another C++ code, into the final control and data flow graph that depicts the total flow of the control and data in the original description. Finally some optional optimization can be applied to meet design constraints in the compilation step.

### 4.4. OPTIMIZATION

Behavioral optimization can be implemented in different ways. It can be applied directly to the parse tree, or during the generation of the intermediate format, or even on the intermediate format itself, according to different cases. Most optimization techniques change control and data flows separately, but some of them affect both flows simultaneously. We use both of these groups in our tool.

The tree-height reduction, constant and variable propagation, common sub-expression elimination and dead code elimination techniques can be applied to data flow graphs. The control flow graphs can be optimized by imposing function flattening and loop unrolling. Another optimization is applied in our tool, which will be useful in next steps (e.g. synthesizing) that combine multiple DFGs to form one single DFG. This optimization affects both CFGs and DFGs, where by increasing the number of operational units in DFG, resource sharing capability increases. This method applies to parallel blocks within sequential bodies like the case blocks of a switch construct or blocks of if-then-else constructs. The complexity of this method is $O(n)$, where $n$ is the number of blocks in the intermediate code of CFG. The effects of these optimizations are verified in next section.

## 5. EXPERIMENTAL RESULTS

For proving the effectiveness of our method for modeling and simulation of asynchronous circuits in SystemC we choose JPEG encoder, which is composed of various blocks and is a suitable case to show the synchronization between modules. All blocks were implemented with our library in SystemC and are connected to each other through asynchronous channels. Table 1 presents the number of SystemC lines of code, number of words and characters. Comments and blank lines in the source are not included in these numbers.

Table 1

Report of JPEG implementation in SystemC

| | #LINES | #WORDS | #CHARECTERS |
|---|---|---|---|
| RGB_2_YCbCr | 53 | 197 | 1226 |
| DCT | 75 | 283 | 1597 |
| Quantization | 53 | 200 | 1267 |
| Zig Zag Scan | 93 | 247 | 1781 |
| Encoder | 128 | 329 | 2207 |
| Entropy Coding | 63 | 143 | 1270 |
| Total | 465 | 1399 | 9348 |

To evaluate our control data graph extraction tool we choose the differential equation integrator circuit. Fig 8. shows its high level asynchronous description with related primary extracted CFG and DFGs with no optimization. Table 2 shows extracted parameters of CFG and DFGs before and after optimization. In this table "Control blocks" is a construction used in CFG. And "operation" is an arithmetic or logical operation that was used in DFGs. In addition to the proposed intermediate representation for DFGs (in Fig 8.c), our tool generates DFGs in a visualized format of dot.

```
DFG;000;
IN;x;w_001;8;
IN;dx;w_002;8;
IN;a;w_004;8;
OUT;f_000;w_005;8;
+ w_003 w_001 w_002
<w_005 w_003 w_004
GFD;
DFG;001;
IN;x;w_006;8;
IN;dx;w_007;8;
OUT;x1;w_008;8;
+w_008 w_006 w_007
GFD;
DFG;002;
IN;y;w_009;8;
IN;u;w_010;8;
IN;dx;w_011;8;
OUT;y1;w_013;8;
*w_012 w_010 w_011
+w_013 w_009 w_012
GFD;
```

(c)

```
DFG;003;
IN;u;w_014;8;
IN;3;w_015;2;
IN;x;w_016;8;
IN;dx;w_019;8;
IN;3;w_022;2;
IN;y;w_023;8;
OUT;u1;w_026;8;
* w_017 w_015 w_016
* w_018 w_017 w_014
* w_020 w_018 w_019
- w_021 w_014 w_020
* w_024 w_022 w_023
* w_025 w_024 w_019
- w_026 w_02 w_025
GFD;
```

```
MOD;0;PI;X;8;PI;Y;8;PI;U;8;PI;DX;8;PI;A;8;AO;Uo;8;
THR;
V_DCL;x;8;
V_DCL;y;8;
V_DCL;u;8;
V_DCL;dx;8;
V_DCL;a;8;
V_DCL;x1;8;
V_DCL;y1;8;
V_DCL;u1;8;
PAR_PAS_READ;0;X;x;Y;y;U;u;DX;dx;A;a;
loop;1;000;IN;x;IN;dx;IN;a;OUT;f_000;
VA;0;001;IN;x;IN;dx;OUT;x1;
VA;1;002;IN;y;IN;u;IN;dx;OUT;y1;
VA;2;003;IN;u;IN;x;IN;dx;IN;y;OUT;u1;
VA;3;004;IN;x1;OUT;x;NULL_DFG;
VA;4;005;IN;y1;OUT;y;NULL_DFG;
VA;5;006;IN;u1;OUT;u;NULL_DFG;
pool;
PAR_ACT_WRITE;2; Uo; u;
RTH;
DOM;
```

(b)

```
#include "asynch.h"
#include <systemc.h>
SC_MODULE(diffeq){
public:
APAS_IN<sc_uint<8>>X,Y,U,DX,A;
AACT_OUT <sc_uint<8> > Uo;
SC_CTOR(diffeq)
{ SC_THREAD(main); }
void main(){
sc_uint<8>  x,y,u,dx,a,x1,y1,u1;
while (true){
PAR_PAS_READ(X,x,
        Y,y, U,u, DX,dx, A,a);
for( ; x+dx<a ; ){
 x1= x + dx ;  y1= y + u*dx ;
 u1= u - 3*x*u*dx - 3*y*dx ;
  x = x1; y = y1; u = u1;
 }
 PAR_ACT_WRITE(Uo, u);
}};
```

(a)

Fig. 8. (a) High-level Asynchronous SystemC of DifEq (b) Extracted CFG (c) Extracted DFGs

Table 2

DifEq before and after imposing optimization

| | BEFORE | AFTER |
|---|---|---|
| Number of Control blocks | 9 | 6 |
| Number of DFGs | 4 | 1 |
| Total Number of operation in DFGs | 12 | 10 |

## 6. CONCLUSION AND FUTURE WORKS

We presented a library to model asynchronous circuits in SystemC language. Limitation of SystemC in modeling asynchronous channels, handling conditional flow

control, and unconditional flow control can be addressed by adding this library to SystemC. Some concepts such as *multi channel to one channel, one channel to multi channel* read/write operations in asynchronous channels were elaborated. Early design modeling and simulation can be done in the first step of the design. Asynchronous SystemC Library constructs were developed with the view of synthesizability of these concepts. Next, an automated tool was presented capable of extracting control and data structures from high level description of Asynchronous SystemC code and optimizing them for synthesis purposes. As future works we will develop our tool to synthesize the extracted constructs into asynchronous circuits, and apply some scheduling, allocation and binding algorithms so that we shall benefit from all advantages of asynchronous circuits.

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# SOI monolithic active pixel detector technology for improvement of I-V characteristics and reliability

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Monolithic active pixel detectors in SOI (Silicon On Insulator) technology are novel sensors of ionizing radiation, which exploit SOI substrates for the integration of readout electronics and a pixel detector. Breakdown voltage and leakage current of pixel diodes are very important parameters of the devices. This paper addresses recent development in the field of the technology of the SOI detectors, which lead to improvement of reliability and current-voltage characteristics of the sensors.

*Keywords:* SOI technology, detectors of ionizing radiation, silicon detector, pixel detector, monolithic detector, active pixel detection

## 1. INTRODUCTION

The main modern trend in sensor technology is to integrate detectors with readout electronics. Such an integrated sensor has usually not only better performance but is smaller, more reliable and more cost-effective. Monolithic active pixel detectors in SOI technology are novel sensors of ionizing radiation which integrate radiation

sensitive substrate diodes with readout electronics in one structure. These sensors find applications in medicine and high-energy physics experiments.

The development of the SOI detectors was started by the collaboration of ITE Warsaw and AGH Cracow in 2001 as a part of the SUCIMA project [1]. The basic structure of the proposed device is given in Fig. 1. The sensor was manufactured using wafer-bonded SOI substrates. The matrix of radiation sensitive junctions was formed in a high resistivity 400 μm thick support layer of a SOI wafer and was separated from electronics manufactured in a device layer by a 1 μm thick buried oxide (BOX). A more detailed description of the SOI detector can be found elsewhere [2].

Very first versions of the SOI detectors suffered from early breakdowns and relatively high dark currents (around 200 nA/cm$^2$) of the sensor junctions located in the high-resistivity part of the SOI wafer. Moreover, the potential distribution in the radiation sensitive substrate could be disturbed by readout electronics. As the p-wells formed in the device layer used to reach the BOX interface, their bias was expected to cause local potential variations in the gaps between pixels [3].

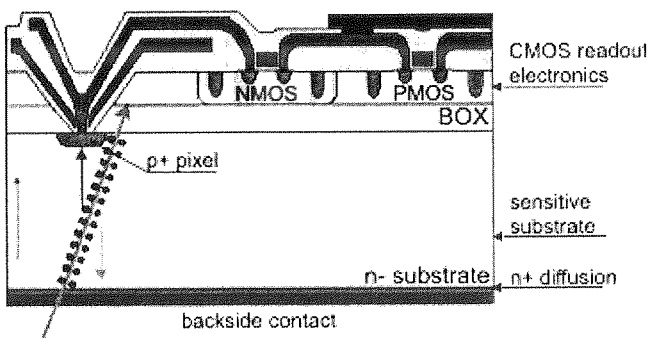


Fig. 1. Cross-section of a monolithic active pixel detector in SOI technology

To overcome these problems, modification of the detector structure and improvement of the quality of starting material and technology was required. The effect of readout electronics bias on the detector operation was minimized by increasing the device layer thickness from approximately 1.2 μm to 4 μm (after device processing). Due to this solution, the well implantations are terminated far from the buried oxide interface and the charge collection in the detector substrate was not disturbed. Also an influence of pixel bias on readout circuitry was much smaller than in the previous technology. In order to reduce the leakage currents of the radiation sensitive junctions, some innovations were made to the device technology and customized SOI wafers provided by NISRC Belfast were used for manufacturing the latest lots of SOI detectors. Details of wafer processing and modifications to the SOI detector technology are described in the following sections.

## 2. SOI SUBSTRATES

The substrates for the latest batches of SOI detectors were fabricated using wafer bonding and grind/polish technology. The target thickness of the device layer was 5 μm and the buried oxide (BOX) layer was 1 μm. The 400 μm thick n-type high resistivity (> 4,000 Ω · cm) FZ <100> handle wafers were supplied by Topsil. The low resistivity (1.5-3.0 Ω · cm) active wafers were n-type CZ <100>, supplied by Siltronic.

Vertical integration of the CMOS electronics with the pixel diodes requires a top quality of electrical interface between the BOX layer and the handle wafer. The 1.05 μm thick BOX layer was grown on the handle wafers using a wet oxidation ('hydrox') process at 1050°C for 3 hours. These substrates were then bonded to the active wafers, followed by a 2 hours bond strengthening anneal at 1050°C. To ensure minimal degradation of the high resistivity properties of the handle wafers, optimized controlled temperature ramps were employed during both wet oxidation and bond annealing. The final 4.5 μm SOI active layer thickness was then achieved by precision grinding and polishing.

The crucially important BOX-substrate interface was examined using test structures with matrices of pixel diodes surrounded by double guardrings and MOS transistors fabricated in 500 nm ion split SOI substrates with similar BOX technology. The latter was also checked for radiation immunity. The results have demonstrated the suitability of the SOI substrates for manufacturing ionizing particle detectors for high radiation environments.

## 3. IMPROVED TECHNOLOGY OF THE SOI DETECTORS

Early technology of the SOI detector used in the SUCIMA project is described in [4]. In order to improve the current-voltage characteristics of the latest lots of SOI detectors, a polysilicon getter layer was deposited on the backside of the SOI wafers prior to the main technological sequence. This polysilicon layer was then heavily doped with phosphorus and it was finally used as a part of the backside ohmic contact. To enhance gettering efficiency, the polysilicon layer was deposited in two separate steps (processes). Additionally, in comparison to earlier experiments, the parameters defining the depth of the back ohmic contact (time and temperature of annealing) were optimized with the assumption that the annealing temperature ought not to be higher than at any other stage of the manufacturing process. Moreover, similarly to the previous innovation, the backside was protected against touching steel parts of technological machinery (which might contaminate the substrate with iron) by a protective layer of silicon nitride. This backside silicon nitride layer and a part of the polysilicon layer were removed just before metal deposition at the very end of the fabrication process. Both these protective procedures, together with use of the customized SOI wafers described in the previous paragraph, completely removed diode early breakdown phenomena and considerably reduced dark currents.

## 4. EXPERIMENTAL RESULTS

The quality of the pixel diodes was assessed using test structures built of matrices of 36 junctions (6 × 6) surrounded by double guardrings. Every test structure consisted of 8 matrices that differed in the layout of the diode and its connection to the readout electronics. Namely, the window in the device layer ranged from 38 μm to 45 μm, the window in the BOX from 18 μm to 24 μm, and the path width from 9 μm to 15 μm. The pixel pitch was 150 μm for all the matrices.

Measurements of the test structures were performed for five wafers coming from two lots. Despite the increase in the device layer thickness, continuous electrical paths over the pixel cavities were obtained for all the structure types and no short circuit between device layer and detector substrate was observed. With reference to previous lots of the diodes produced on SOI substrates, significant improvement of the I-V characteristics was achieved. Breakdown voltages higher than 100 V were obtained for 70 % of test structures from the first lot and for 98 % of test structures from the second lot, as shown by the typical diode reverse I-V characteristics given in Fig. 2. The leakage currents of reverse biased junctions were also significantly reduced. The lowest values of leakage current were measured for the matrix with the smallest pixel width. Normalized diode leakage currents measured at a reverse bias voltage of 70 V for various positions over one of the wafers are presented in Fig. 3, showing an average value of only 55 nA/cm$^2$.

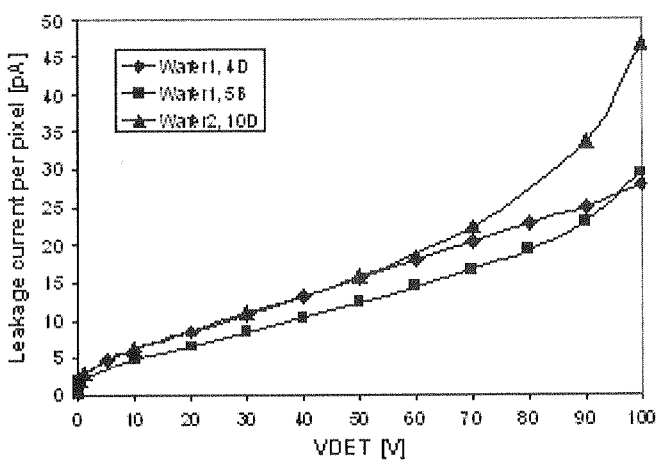


Fig. 2. Typical I-V characteristics of pixel diodes

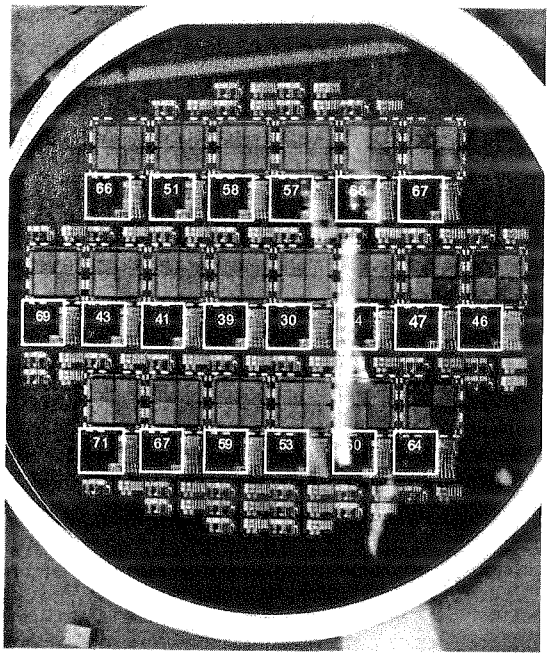


Fig. 3. Leakage currents in nA per $cm^2$ measured at 70 V

## 5. CONCLUSIONS

The technological aspects of the development of improved monolithic active pixel detectors exploiting SOI technology have been described. The effectiveness of the recent technology modifications was demonstrated by the measurements of the characteristics of the radiation sensitive junctions. Recent results in the field of the SOI detectors indicate that the SOI technology allows for manufacturing of high quality ionizing radiation sensors. Further development of the detectors involved tests of the matrices of complete, fully integrated and was reported in [5] devices.

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# Experimental study of power IGBT technologies at large range temperature

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Aeronautical power electronics applications impose high power density handling and device operation temperatures. SiC technology not being mature enough, the temperature limits of silicon devices must be pushed in order to increase current ranges and the amount of switched power. Device ageing is accelerated and there exist the risk of catastrophic failure by thermal runaway. In order to design correctly high temperature power systems, knowing the IGBT characteristics at extended temperature ranges (-55°C, +175°C) becomes essential. The present work describes an experimental setup and test procedure conceived to experiment with different available IGBT technologies at temperatures above the limits rated by manufacturers. The aim is to generate experimental data for the creation of accurate models with large temperature scale. This will ease prototyping for future development of IGBT modules in aircraft.

*Keywords:* power electronics, characterization, aeronautics, test bench, high temperature, low temperature, IGBT, experimental study

## 1. INTRODUCTION

The More Electrical Aircraft (MEA) pushes the aeronautical industry to interest in power electronics. Electrical energy becomes more and more present in aircraft in

spite of the three other main energy types: hydraulics, mechanics, and pneumatics. Consequently, the study of power electronics system under harsh thermal environment related to aeronautics applications is essential.

The use of power Insulated Gate Bipolar Transistor (IGBT) has largely expanded in the last decades. IGBT devices have become the most convenient device for medium voltage and current applications range thanks to its good trade-off between switching speed, on-state voltage drop and ruggedness. Researches in the field of power semiconductor technology are continuously improving switches, increasing the blocked voltage, the switching frequencies, current density, On-state characteristics [1] and searching to decrease switching energy losses without degrading On-state performance [2]. Silicon Carbide [3] presents many favourable properties to produce devices for high temperature operation (up to 600°C), high frequency and high power applications. However, the use of this remarkable material encounters important technological problems to be solved before high power SiC devices can be commercially available. Thus, as SiC technology is not still mature, it is still worth to push the limits of silicon devices.

As the switched power increases, the silicon junction is submitted to higher temperatures and the device ages faster. The physical properties of the semiconductor changes; the most significant is the considerable reduction of the carrier mobility. The main drawback of IGBT devices at high temperature is the enlargement of its inherent current tail during turn-off. The current tail is responsible of the turn-off losses in the device. The degradation of the device performances can give rise to thermal instabilities during switching operation that can lead the IGBT to catastrophic failure.

In this context, the knowledge of IGBT performances and detailed electrical characteristics at extended temperature becomes essential to system designers. Developing of device models at these temperatures will permit to increase system reliability. Thus, it is necessary to dispose of an experimental facility, adapted for the thermal characterization of power devices at high temperature.

In literature many experimental studies are dedicated to explore the possibility of increasing the junction temperature limit, beyond the limits established by manufacturers, in order to increase power capabilities. Most of them are focused in different ways on the study of the enlargement of current tail at high temperatures due to increased carrier lifetime. These thermal behaviour studies suggest that it is actually possible to operate at high junction temperature avoiding thermal instabilities depending on the device technology and the switching conditions.

Sheng [4][5] experimentally searches the limits of operating temperature of Punch-Through and Non-Punch-Through IGBT technologies at high frequency. The NPT device remains stable above its temperature rated limits (150°C) and it is much less sensitive to temperature changes than PT structure. The upper temperature limit is found to be 230°C for the NPT technology. Thermal runaway has been observed for PT devices, even below 150°C when operated at very high frequency.

Comparative experiments of PT-IGBT and NPT-IGBT structures at high temperature can be found in [6], [7] and [8] with equivalent conclusions. The current tail,

product of the stored charge, enlarges notably with temperature in PT devices, and turn-off losses increase non-linearly. NPT-IGBT is quite insensitive to temperature increase in terms of thermal stability due to the fact that turn-off losses increase linearly. On the other hand, no fundamental differences have been found in turn-on behaviour between these two technologies.

Trench technology with local lifetime control is also tested in [9] and [10] at high and low [11], [12] temperature. Trench structure merits are higher current density, larger ability against latch-up, lower on-state and better trade-off On-state/turn-off losses than a conventional planar device.

## 2. OBJECTIVE

The present work describes an experimental setup and test procedure conceived to experiment with commercially available silicon device technologies at temperatures above the limits rated by manufacturers.

The most rugged devices are going to be used in the power module prototypes for aeronautics applications. The aim of the test bench is to obtain accurate current and voltage waveforms from the power components. Exploration of the power system behaviour at large range temperature will serve to obtain in one hand, a large database of the components performances, and on the other hand, concerning high positive temperature, the possibility of reducing size and weight of the cooling system (for the same power) or to increase the switched power for the same package characteristics, depending on the results. For the study we choose two of the latest IGBT technologies components: the Trench-IGBT and the planar SPT IGBT. Conclusions about the technology that better withstands an extension of its junction temperature range at typical switching conditions of aeronautics applications are searched experimentally. Finally results from these experiments and prototyping experience will allow a detailed analysis and the creation of stored charge models for future technology modifications for high and low temperature operation. Trench characterization has been realised and results concerning this component are presented in this paper. Experimental work concerning the SPT component has started recently.

## 3. EXPERIMENTAL FACILITY

The experimental facility is conceived to measure $I_{ak}$ and $V_{ak}$ transient behaviour during turn-on and turn-off (current tail) as well as On-state, blocking voltages and leakage current. All these parameters extracted at different device temperatures. The facility is constructed in the Power Electronics Associated Research Laboratory (P.E.A.R.L) in Tarbes (France).

## 3.1. ELECTRICAL SETUP

### *3.1.1. TEST DEVICE DESIGN*

Test devices (Fig.1) are composed of AlN substrates, metal-coated on double faces, on which are soldered the IGBT or diode die chips. For mainly mechanical reasons, the substrates are fixed on a copper baseplate. Finally, a plastic material structure is added in order to encapsulate a silicone gel for the dielectric aspect as well as power and signal connections for electrical measurements.

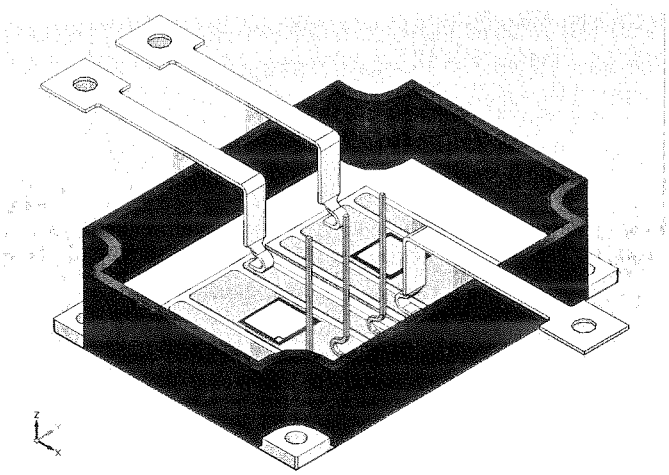

Fig. 1. C.A.D. of the test device for general characterization

The test device is built around the die and the "internal layout" is realised by wire bonding and according to a chopper cell circuit configuration (Fig.2).

Two different test devices and test circuits are used for the electrical characterization of the IGBT components and the PiN diodes. For the PiN diode test device, the electrical configuration of the circuit is the same as for the IGBT configuration test circuit, except for the position of the loop inductance. Indeed, in order to measure the current going through the diode, the inductance is placed between the IGBT emitter and the negative potential of the electric circuit (Fig.3), creating a loop with the diode and the shunt resistance.

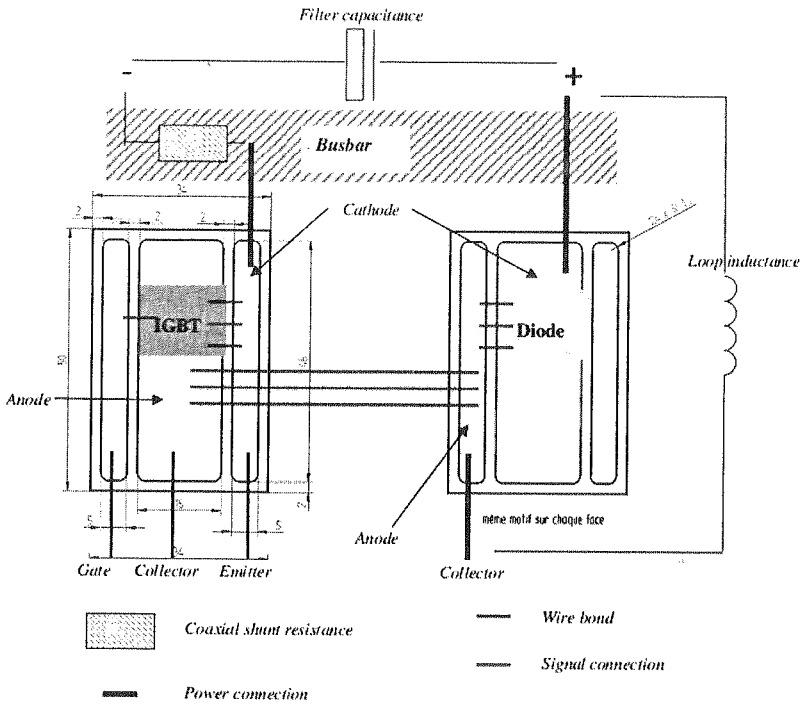


Fig. 2. Layout of the test device; IGBT test configuration

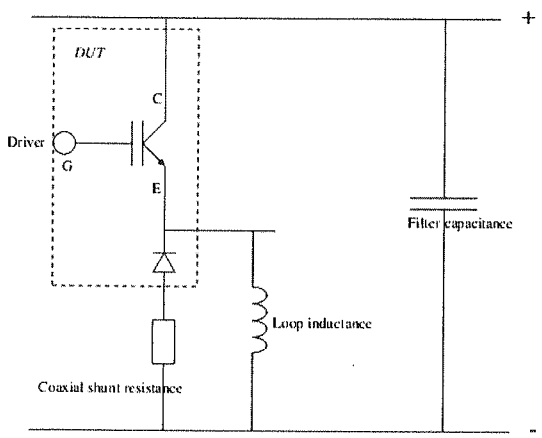


Fig. 3. Diode test circuit configuration

Test devices are realised in a white chamber. There are two main steps in the assembling of these power modules. Firstly, the dies are soldered on the substrates, and in a second step, substrates and connections are soldered on the baseplate and on the substrates respectively. For this process the setting up of specific tools are necessary (Fig.4) and operate as process masks.

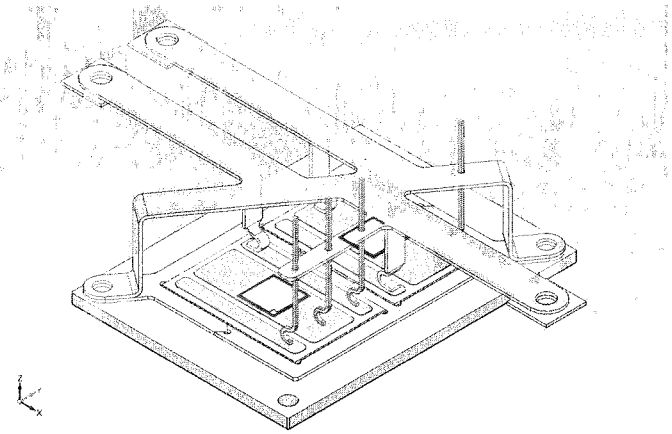

Fig. 4. Tools process for the test device

### 3.1.2. STATIC SETUP

The global view of the test bench for the static characterization can be seen in Fig. 5. Explanation about the use of the Thermostream airflow is provided in the next chapter concerning the thermal setup.

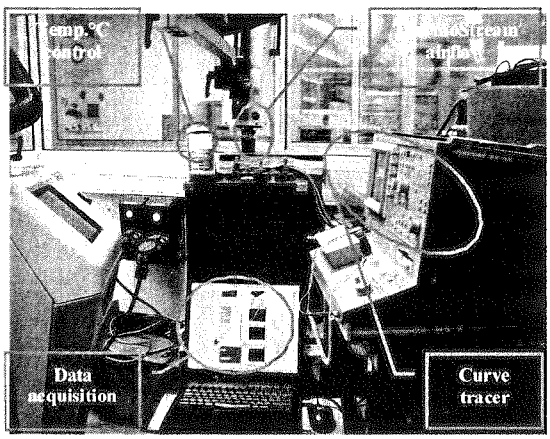


Fig. 5. Global view of the static test facility

The test device is used for the static operation mode. Thanks to a high power curve tracer TEKTRONIX 371A, we are able to make electrical measurement such as Ice (Vce) and breakdown voltage. For the on-state curves we measure the characteristics varying the command gate voltage. The equipment is commanded by a software program developed with Labview®. Power cables are used to connect the curve tracer with the test device inside the temperature chamber.

### *3.1.3. DYNAMIC SETUP*

As for the previous part, a global view of the facility for dynamic characterization is shown in Fig. 6. Once more explanation about the use of the Thermostream airflow is provided in the next chapter concerning the thermal setup.

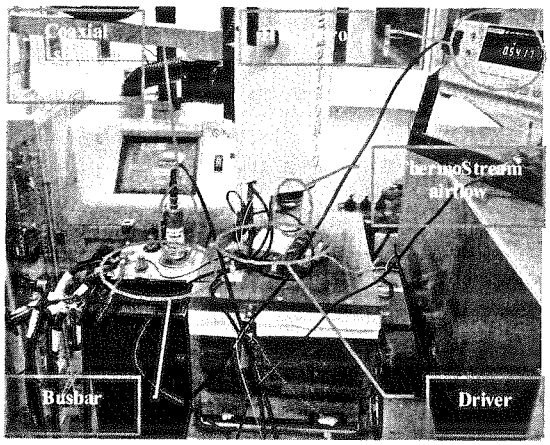


Fig. 6. Global view of the static test facility

A chopper cell configuration is used to characterize the power components (Fig.7). The power voltage source, that charges the filter capacitance, is a high voltage Technix CCR series 5kV equipment, used for the railway tests operations. The High Voltage supplying the circuit is controlled permanently by a HV probe Fluke 80K-6 and a multimeter.

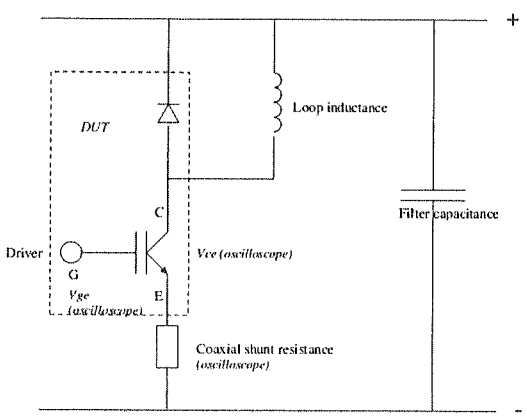


Fig. 7. Dynamic test circuit

The Ice current signal is measured on a TEKTRONIX TDS7054 oscilloscope with the help of a coaxial shunt resistor. For the gate command, a Semikron® SKHI 22B

IGBT driver and a low frequency HP33120A generator are used. The IGBT driver is commanded by a software program developed with Labview® software.

The Vge signal is measured by a differential probe TEKTRONIX P5205, the Vce signal is also measured by a HV differential probe TEKTRONIX P5210. If necessary, the current signal across the loop inductance can be obtained from a Rogowski probe and visualised on the oscilloscope.

The electrical power distribution of the circuit is realised with the help of a busbar (Fig.8). The basic busbar consists of the superposition of two copper sheets creating two conductors nearby. The aim is to reduce the value of the inductance significantly in comparison with the use of power cables. In this case we designed a specific busbar according to simple rules in order to optimize our system [13].

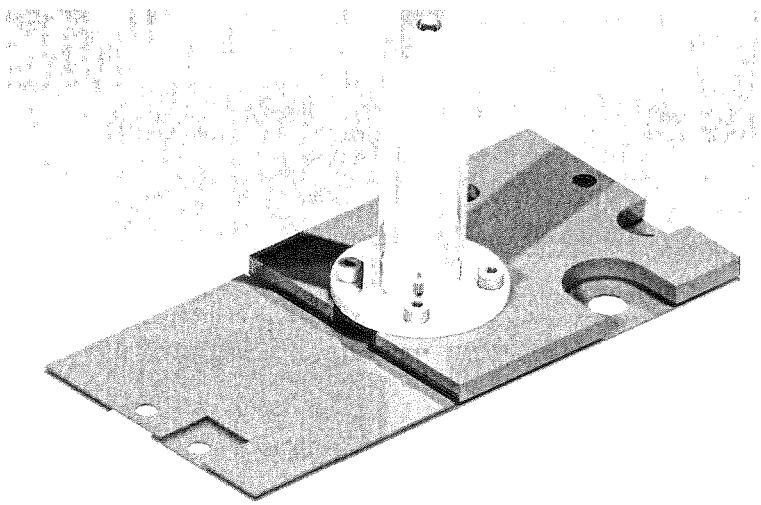

Fig. 8. C.A.D. of the busbar with the shunt resistance

The transient response of Ice and Vce during commutations turn-off and turn-on is measured. These curves provide valuable details about the device switching and the effects of temperature. Especially interesting is turn-off and turn-on losses variation with temperature.

### 3.2. THERMAL SETUP

The active power devices under test must be maintained at controlled temperature. Also, self-heating due to operation during tests must be minimized by giving the heat an easy thermal path, with minimum thermal resistance to evacuate. Devices under test are mounted on small metallised ceramic substrates. Both substrates are sold on a Cu baseplate which temperature is fixed by airflow of constant temperature at its bottom. The DUT (Device Under Test) is then mounted on a specific device designed in order to collect the airflow and share it homogeneously at the bottom of the baseplate. The

whole assembly is placed into a thermally isolated box, where the flow will recirculate in order to keep surrounding air at the wanted temperature. The principle is shown schematically on Fig. 9.

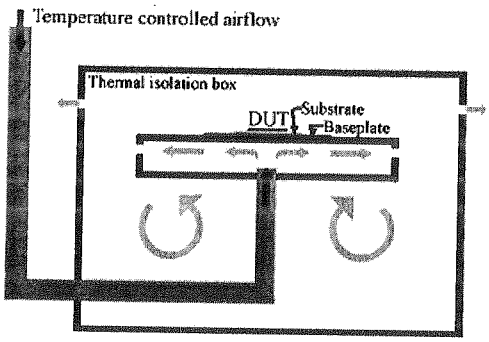


Fig. 9. Principle of the thermal setup

The temperature-controlled air is injected by a ThermoStream® TEMPTRONIC TP04300 (an instrument for thermal characterization of components) that is connected to an entry point. An ensemble of thermocouples (T type) is placed on the baseplate in order to keep the actual substrate temperature monitored. This lecture will give also feedback to the ThermoStream®, which will vary the airflow to attain the correct temperature. Fig. 10 shows the cavity design, with the DUT mounted and the external box design.

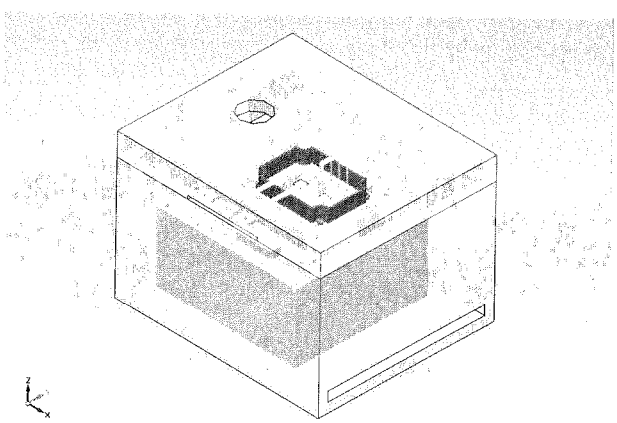

Fig. 10. View of the thermal device with the DUT

The main criterion for the design of the airflow path was simply to integrate it as much as possible. The aim in doing it was to limit thermal losses during the airflow transit. The first design for the thermal device integrated the airflow path into one piece in metal material. However thermal simulation shown that the temperature were not

homogeneous on the test device. In order to solve this problem we performed fluidic simulation (Fig. 11).

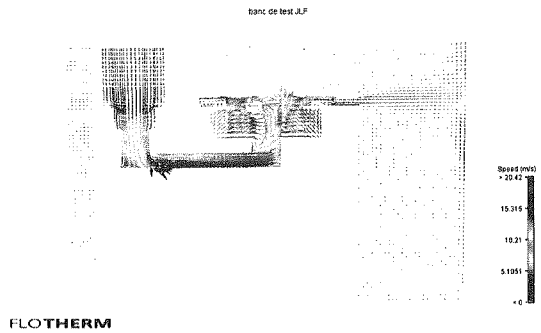


Fig. 11. View of the thermal device with the DUT

Consequently, one can see that on this simulation, the sharing of the airflow at the bottom of the test device is not sufficiently balanced. The bad thermal sharing is linked to the bad airflow distribution. Another problem is the intensity of the airflow inside the device that can reach more than 20m/s. This can lead to an ejection of the ThermoStream® because of the pressure generated. As a consequent we optimized a second design of our thermal device regarding data we got from the previous study. Computational Fluid Dynamic simulations have been performed with FLOTHERM® software in order to validate the whole thermal assembly. This shows that temperature is homogeneous on the baseplate and on the devices, and equal to the wanted temperature. Fluidics simulation (Fig. 12) shows a good behaviour of the whole thermal system, that impacts on the optimization of the convective exchange coefficient, and consequently on the thermal response time for the electrical tests.

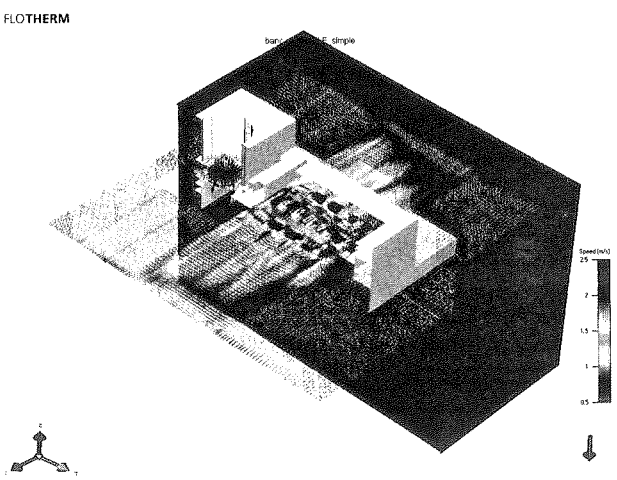


Fig. 12. Fluidies simulation of the thermal system

## 4. EXPERIMENTAL TESTS AND CONDITIONS

### 4.1. STATIC MODE

We performed On-state characterization as well as breakdown voltage measurement for different temperature steps as shown in Table 1.

Table 1

Static test conditions

| | |
|---|---|
| Positive Temp. [°C] | 27; 50; 75; 100; 125; 150; 175 |
| Negative Temp. [°C] | 0; -15; -25; -35; -45; -55 |
| Gate voltage [V] | 11; 13; 15; 17 |

In this part, the temperature was an important changeable parameter; we also measured on-state curves for different levels of gate command voltage.

### 4.2. DYNAMIC MODE

For the switching characterization, we used several parameters that are resumed in Table 2.

Table 2

Dynamic test conditions

| | |
|---|---|
| Positive Temp. [°C] | 27; 100; 125; 150; 175 |
| Negative Temp. [°C] | 0; -25; -40; -55 |
| Gate resistance: on,off [Ω] | 5Ω |
| Voltage [V] | 540 |
| Ice Current levels [A] | 50; 100; 150 |
| Loop inductance [μH] | 300 |

We performed turn-off and turn-on characterization versus the temperature for the IGBT test configuration and the turn-off phase characterization for the diode test.

## 5. RESULTS AND DISCUSSION

Some characterization work has been done and main parameters are presented.

### 5.1. STATIC CHARACTERIZATION

We measured the basic On-State curve as shown on Fig. 13. For the presented curve the gate supply is setup to 15V. One can analyse the effects of the temperature on the component output characteristics.

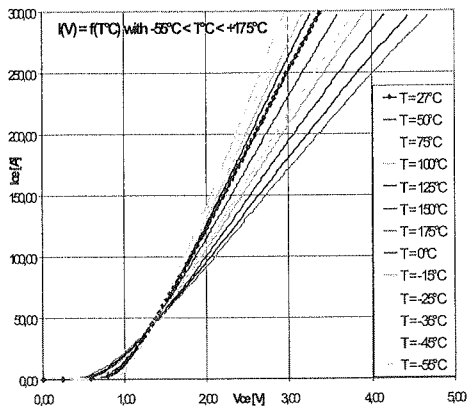


Fig. 13. Ic(Vce) versus temperature @Vge = 15V

The studied Trench IGBT presents a cross point on the static characteristics. Above this point equal to about 40A, the component presents a positive temperature coefficient of the $Vce_{sat}$. The increase of the temperature induces an increase of the electrical resistance (for a same Vce, the collector current decreases with the increase of the temperature). This can be explained by the rising evolution of the intrinsic concentration with temperature and thus, the decreasing of the carrier mobility. Inversely, below the cross point, the IGBT presents a negative temperature coefficient of the $Vc_{esat}$ (for a same Vce, the Ice current increases with the increase of the temperature). In this part of the curve, the carrier mobility becomes a paramount parameter. The decrease of the electrical resistance is due to the enhanced injection across the P-N junction with the increase of the temperature. These simple conclusions can be important when paralleling the power components. Indeed, negative temperature coefficient can lead to a thermal runaway if the sharing of the heat between the active components is not optimized. On the contrary, positive temperature coefficient ensures homogeneous current distribution between components consequently allows easy paralleling and leads to a stabilization of the thermal.

Forward blocking voltage was also investigated. Fig. 14 shows the evolution of the Breakdown Voltage versus the temperature. One can observe that the BV increases

when the temperature increases as well. This is related to the decrease of the ionisation coefficients representing the rate of ionizing collisions of each carrier charge. It can be seen that at ambient temperature (27°C) the breakdown voltage is around 1420 V. This is a good order of value considering that the component is a 1200V voltage rating and that manufacturers plan in general a 20% margin when designing components. However at high temperature, although the blocking voltage is higher, one important disadvantage is the increase of the leakage current. Indeed, the high growth of this current can lead to a thermal instability. In Fig.14, curves at temperature levels 125°C, 150°C and 175°C are not represented due to the high difference in the current values. Even if the leakage current can not be seen in this figure, going from one extreme temperature to the other the current can vary until three orders of magnitude.

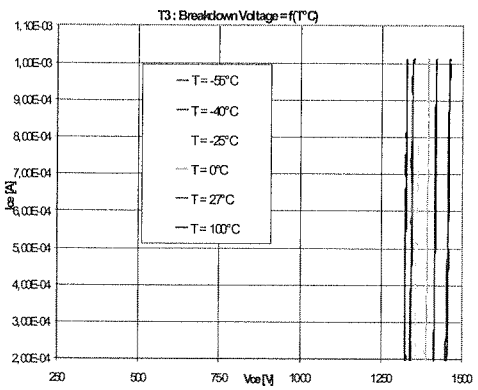


Fig. 14. Breakdown Voltage vs Temperature [°C]

## 5.2. DYNAMIC CHARACTERIZATION

Since the evolution of the temperature will influence the thermal sensitive parameters, this will as well influence the component behaviour. Figure 15 shows the turn-off switching for various temperatures at a load Ice current of 150A. The most important parameter here is the current tail that impacts directly on the switching losses. Due to an injection of minority carrier in the storage region of the component, the IGBT needs to evacuate totally the charges before being able to block the voltage again. Thus the carrier lifetime is an essential parameter. Carrier lifetime is a sensitive parameter with the temperature and depends a lot on the level of injected recombination centers. Indeed many processing methods exist in order to control the lifetime of the carrier going from thermal diffusion of impurity to the use of high energy radiation technique. It has been found that the lifetime of minority carriers in the drift region increases when the temperature increases.

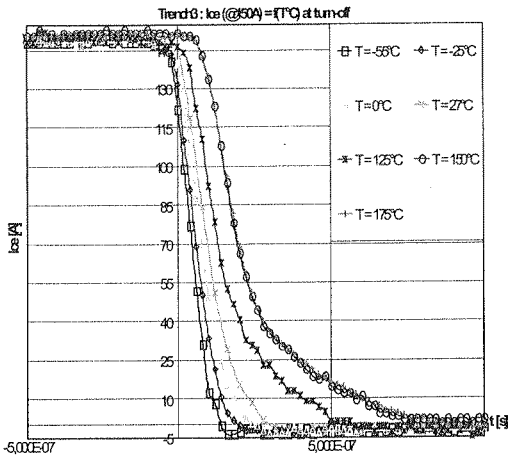


Fig. 15. Turn-off (@Ice = 150A)

It can be observed that at the low temperature, the carrier lifetime is not as strongly influenced as for high temperature. Fig. 16 shows the fall time evolution of the Ice current during turn-off and the Vce voltage at turn-on phase, both curves versus the temperatures. Ice fall time curve confirms the previous result concerning the current tail. One can observe that the Ice fall time curve increases drastically with the high temperature. In fact the value can be multiplied by four times in comparison with the result obtained at very low temperature.

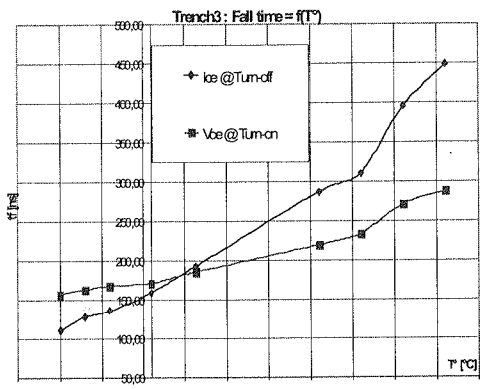


Fig. 16. Turn-off (@Ice = 150A)

The over-voltage has also been measured (Fig. 17) still during the turn-off phase. The decreasing amplitude of the over-voltage (Fig. 18) as well as the decrease of the voltage slope dV/dt are pointed out.

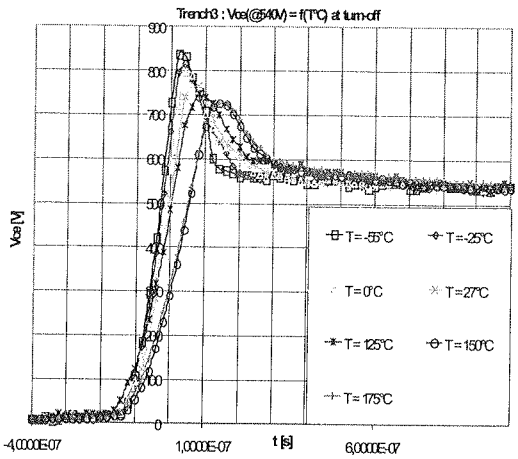


Fig. 17. Vce curve @ turn-off (@Ice = 150A)

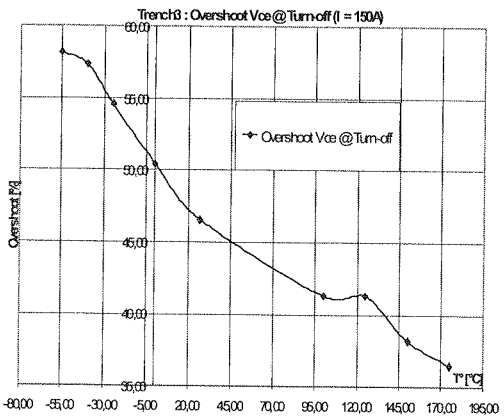


Fig. 18. Vce overshoot @ turn-off (@Ice = 150A)

As we expected the over-voltage decreases slightly from around 830V to around 720V for a load current of 150A and a supply voltage of 540V. This phenomenon is linked with the LdI/dt quantity that diminishes because of the carrier lifetime growth with the high temperature.

As previously for the fall time, it is possible to evaluate the rise time of the current and voltage of the component (Fig. 19).

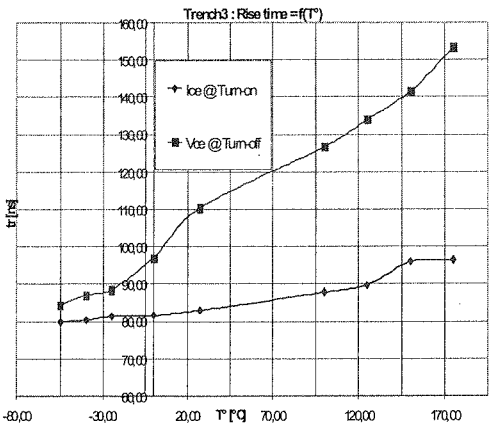


Fig. 19. Rise time vs temperature (@Ice = 150A)

The Ice rise time is not as influenced by the temperature as the Vce tr is during turn-off phase. Indeed as we have seen on Fig. 17, the dVce/dt parameter varies significantly. In order to link the two curves, it can be observed that in a general way, more the slope of the dVce/dt is high more the over-voltage is. These data are essential for system designer in order to prevent failure mode considering EMC aspect notably at high frequency or RBSOA limit definition.

In order to fully characterize the component the energy curves during turn-on and turn-off phases have been calculated. We can observe the evolution of the curves on Figs. 20 and 21. These values are given for the intrinsic characteristics of the component with an inductive load for each switching cycle in order to calculate the global power dissipation. Once more, one can notice that the curves don't evolve the same way going from ambient temperature to high or low temperature. Focusing on the Eoff, losses grow faster when going to high temperature than when going to low temperature. With an approximate calculation and taking the 27°C level as a reference it can be found that the Eoff increases by around 0,07mJ/°C for the high temperature when Eoff decreases by around 0,046mJ/°C for the low temperature.

Concerning the Eon one can observe that the amplitude of the curves is smaller than for the Eoff curves. This can be explained by the fact that during turn-off we have to take into account the current tail as well as the over-voltage, when during turn-on phase the current overshoot is the only critical parameter. Regarding the evolution of the curves versus the temperature, same report as for the Eoff can be made. With an approximate calculation still taking the 27°C level as a reference, Eon can be found to grow by around 0,029mJ/°C going to high temperature when it decreases by around 0,01mJ/°C going to low temperature.

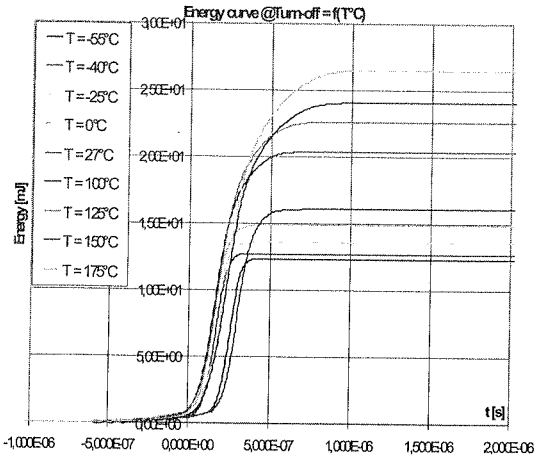


Fig. 20. Energy curve @ turn-off (@Ice = 150A)

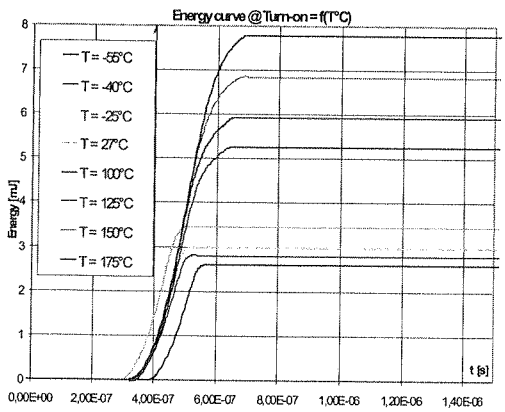


Fig. 21. Energy curve @ turn-on (@Ice = 150A)

Diodes characteristics have also been investigated. Fig. 22 shows the evolution with temperature of the peak reverse recovery current. This characteristic of the PiN rectifiers is an important parameter that induces an additional amount of current in the transistor power dissipation during its turn-on phase. Consequently it degrades the reliability of the component. Reverse recovery current occurs when switching from on-state to reverse blocking state. Just like the IGBT during turn-off, PiN diodes need to evacuate the amount of carriers accumulated in its i-region during forward conduction prior being able to block the voltage again.

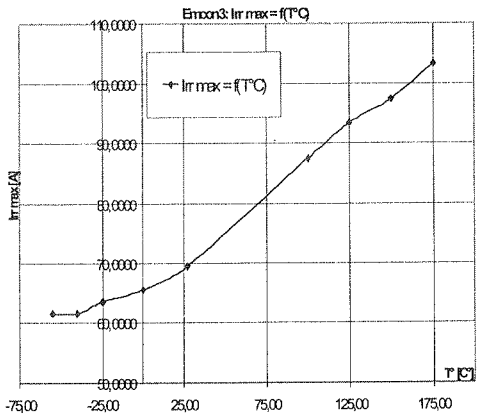


Fig. 22. Recovery current @ rturn-off (@Ice = 150A)

These charges are removed with the help of two phenomena: first a large reverse current flowing through the diode component and in a second time by recombination. It has be found that the peak reverse current (for a 150A load current) varies from 61A at – 55°C to 103A at +175°C. One can notice that the evolution of the curve is relatively linear. Another important point is the reverse recovery time (Fig. 23). This curve indicates the total time that the PiN rectifiers need to entirely recover its blocking power. The Irr waveform (not represented in this paper) reminds the current tail waveform of the IGBT seen previously, in the way of the tailing phase especially for high temperature. The recovery phenomenon leaded by recombination process (because of the bipolar nature of the component) is very sensitive with the positive temperature.

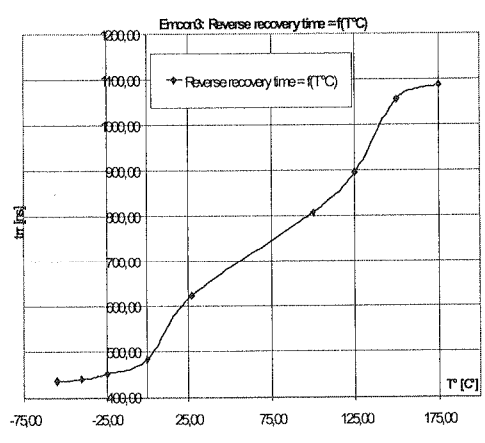


Fig. 23. Reverse recovery time @ turn-off (@Ice = 150a)

Thus the trr is not so far influenced by the low temperature and only vary in a range of 50ns going from -55°C to 0°C. On the contrary the slope increases significantly when going in the positive temperature rising by around 30% at ambient value. The

growth is then relative linear although we can observe that from 100°C the slope becomes higher. Globally the trr can vary more than double when going from one extreme to the other. To roughly resume the Irr max value as well as the trr value will limit the frequency use of the system. Frequency impacting on the dI/dt related to the peak reverse current and the power dissipation.

Thanks to the test bench we designed main electrical characteristics of the components have been investigated allowing a FBSOA and RBSOA limit definition.

## 6. CONCLUSION

Main electrical investigations, results and analysis of power components are presented in this paper. Moreover, an experimental setup is presented and shows that the design of the electrical aspect allows, from a basic test circuit configuration, to obtain essential characteristics of the IGBT and diode power components. Moreover, fluidics and thermal simulation permit to design a facility that eases the electrical test versus temperature by optimizing the convective exchange coefficient and the thermal response time.

Some characterization work is presented in this paper. Static characterizations as well as dynamic characterization have been performed on the Trench IGBT and show the IGBT dependency with temperature on a large temperature range (-55°C; + 175°C).

This test procedure has been done for the Trench IGBT and the PiN rectifier but is also valuable for all types of power IGBT and power diodes. This has permitted an extended experimental study of our components.

## 7. ACKNOWLEGMENTS

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## 9. ADDITIONAL INFORMATION

The authors work with the P.E.A.R.L (Power Electronics Associated Research Laboratory), located in Tarbes, FRANCE, and with the L.A.A.S (Laboratoire d'Analyse et d'Architecture des Systèmes) located in Toulouse, FRANCE. The LAAS laboratory is also related to the University of Paul Sabatier Toulouse 3, Toulouse, FRANCE. Hispano-Suiza Company is a systems integration-engineering firm for the aeronautical industry, and got many industrial sites. The one in partnership is located in the REAU site, FRANCE.

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# FPGA implementation of a lossless to lossy bitonal image compression system

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This paper presents an FPGA implementation of a lossless to lossy image compression system that incorporates region of interest processing. Block Arithmetic Coder Image Compression is combined with Low-Latency Greedy Flipping Utilizing Forgetful Error Diffusion for loss introduction. The approach allows for perfect quality, associated with lossless compression, or three levels of reduced image quality, high, medium and low, associated with various levels of loss introduction. Region of interest processing can be incorporated by adjusting the system parameters for maximum visual benefit. The overall system was successfully realized on a Virtex FPGA platform.

*Keywords:* FPGA, bitonal compression, block arithmetic coder, region of interest

## 1. INTRODUCTION

Near lossless or visually lossless compression requires the introduction of loss without visual distortion. This is particularly challenging when dealing with bitonal images, since changing the value of a pixel is always visible and results in lossy compression. Near lossless compression in bitonal images is desirable and was examined for error diffused images in [1]. In this paper, we present a lossless to lossy image compression system with region of interest (ROI) processing that is amenable to implementation on Field Programmable Gate Array (FPGA) platforms. Lossless compression is based on Block Arithmetic Coding for Image Compression (BACIC) [2] instead of the less effective CCITT Group 3 (G3) [3] and Group 4 (G4) [4] methods or the more complicated JBIG [5] and JBIG2 [6].

## 2. LOSSLESS ARITHMETIC CODER

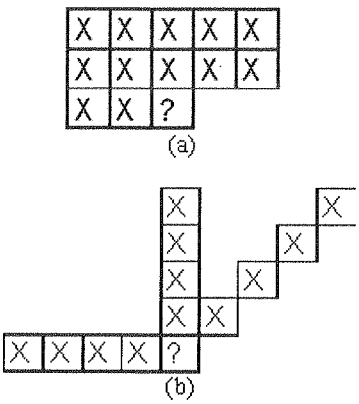


Fig. 1. BACIC Templates (a) 3-line (b) 5-line; '?' denotes current pixel and 'X' denotes context pixel

The BACIC method utilizes a Block Arithmetic Coder [2], which is a simple and efficient coder that is suitable for hardware implementation As is done in the JBIG standard [5], BACIC uses two 12-pixel templates (Figure 1) to estimate the dynamic probabilities $p_0$ and $p_1$, the probabilities that a pixel is 0 or 1 respectively. The three-line template is used for document images or halftones generated by error diffusion, while the five-line template is used for halftones images generated by ordered dither. The pixels of the template are grouped to form an integer, which is a context into a table. The probability is estimated using a table that consists of two real numbers, $r_i$ and $s_i$, as follows:

$$p_1 = \frac{r_i + \Delta}{s_i + 2\Delta} \tag{1}$$

where $i$ is the context, and $\Delta$=0.006 is a constant used to prevent overestimating $p_1$. The quantities $r_i$ and $s_i$ are

$$r_i(n+1) = u + \alpha \cdot r_i(n) \tag{2}$$

and

$$s_i(n+1) = 1.0 + \alpha \cdot s_i(n) \tag{3}$$

where $r_i(0) = 1.0$, $s_i\ (0) = 2.0$, $u$ is the value of the current pixel and $n$ is the number of previous pixels having context $i$. The constant $\alpha$ is the forgetting factor ($\alpha$=0.985), used so that recent pixels have a more significant effect on $p_1$. The block arithmetic coder uses a binary coding tree to determine the codeword for a variable set of pixels. The arithmetic coder uses two parameters, $p_0$ and $K$, to perform the encoding. Note that $p_1$ =1-$p_0$ and $K$=4096 is a power of 2 equal to the size of the BAC codebook.

During encoding, the image is traversed in raster scan order and for each pixel $p_1$ and $p_0$ are computed. Then $K_0$ and $K_1$ are found using

$$K_0 = round(K \cdot p_0) \tag{4}$$

and

$$K_1 = K - K_0 \tag{5}$$

A tree is built with parent node $K$ and two child nodes $K_0$ and $K_1$. Depending on the current pixel, either $K_0$ or $K_1$ is chosen as the new parent node and the process repeats until a value of 1 is obtained. When encoding an image, the probabilities change as the template moves and the $r_i$ and $s_i$ values change, which warrants the use of an adaptive tree. This is the process used in the BACIC algorithm, with the exception that a much larger $K$ value is used to yield better compression results. The next section presents a method for introducing loss into the image.

## 3. LOSS INTRODUCTION METHOD

Changing pixel values, or pixel flipping, in a bitonal image is performed in a manner that decreases the overall encoding length of the image. To introduce loss in combination with BACIC, the forgetting factor $\alpha$ in (2) must be ignored, since the image is processed as a whole. Therefore, $\alpha$ is set to 1.0 and

$$r_i(n+1) = u + r_i(n) \tag{6}$$

and

$$s_i(n+1) = 1.0 + s_i(n) \tag{7}$$

Thus, $r_i$ counts the number of previous pixels for each context that equal '1', while $s_i$ counts the number of previous pixels for each context. For the loss introduction portion, let $n_0(c)$ and $n_1(c)$ denote the number of pixels for context $c$ equaling a '0' and '1' respectively to obtain:

$$p_1 = \frac{n_1 + \Delta}{n_0 + n_1 + 2\Delta} \tag{8}$$

and

$$p_0 = 1.0 - p_1 = \frac{n_0 + \Delta}{n_0 + n_1 + 2\Delta} \tag{9}$$

Since the values for $p_0$ and $p_1$ are found using templates, flipping a pixel, $u$, changes both the encoding length of itself and the encoding length of all the pixels for which $u$ is a template pixel. The quantity $\Delta L_q$ denotes the impact on the code length

when altering the context of the pixel for which $u$ is context pixel number $q$. The change in code length of the entire image, $\Delta L$, when a pixel is flipped is:

$$\Delta L = \sum_{q=0}^{k} \Delta L_q \tag{10}$$

where $k$ is the number of pixels in the context, i.e. for BACIC, $k$=12. The direct gain from flipping $u$ to $\bar{u}$ in context c is [2]

$$\Delta L_0 = \log_2 \frac{n_u(c) - 1 + \Delta}{n_{\bar{u}}(c) + \Delta} \tag{11}$$

Using the notation $u'$ as the value of the mirror pixel of context pixel number $q$, the indirect terms in the sum are

$$\Delta L_q = \log_2 \frac{n_{u'}(v_q) - 1 + \Delta}{n_0(v_q) + n_1(v_q) - 1 + 2\Delta} - \log_2 \frac{n_{u'}(w_q) + \Delta}{n_0(w_q) + n_1(w_q) + 2\Delta} \tag{12}$$

where $v_q$ is the original context for pixel $q$ and $w_q$ is the context for pixel $q$ if the pixel $u$ is flipped [2]. The rest of this section discusses how to use the values $\ell$ and $\Delta L$ to determine which pixels should be flipped.

### 3.1. LOW-LATENCY GREEDY FLIPPING UTILIZING FORGETFUL ERROR DIFFUSION

The algorithm used for the introduction of loss is Low-Latency Greedy Flipping Utilizing Forgetful Error Diffusion [2], which provides effective means for controlling image quality and is suitable for hardware implementation. It requires two passes over the entire image, one to collect statistics over all contexts, and another to flip pixels. In the first step, the context for each pixel is found and either $n_0$ or $n_1$ is incremented depending on the pixel value. During the second step, the image is divided into blocks of size 8×8 pixels. Each block is processed in raster scan order, $\Delta L$ is computed for each block pixel, and, if distortion control allows it, the most profitable pixel is flipped. If distortion control does not allow it, the second most profitable pixel is flipped and so on. The parameter $n_{max}$ is the maximum number of times each block can be processed. Since only one pixel is flipped on each pass of a block, $n_{max}$ is also the maximum number of pixels that can be flipped in each block. It is desirable to make $n_{max}$ an even number, to allow for complementary flips that maintain the average block intensity. The perceived grayscale error for each image block is the main distortion controlling quantity, but a limit $g_{max}$ is set on the grayscale error per block. After processing a block, its grayscale error is diffused to the other surrounding blocks using the Floyd-Steinberg weights [5]. Complementary flips, either in the same block or in neighboring blocks, are desirable because they maintain the overall perceived grayscale quality of the image. The $s$ parameter is a scaling factor between 0.0 and 1.0 that is used when diffusing the error. When no flips can be done in a block, the grayscale

error for that block is multiplied by $s$ before diffusing. This is an important parameter for the quality of the image, because it can reduce the amount of recorded grayscale error diffused and allow more pixels to be flipped. The thresholds $\tau_L$ and $\tau_\ell$ are used to check against $\Delta L$ and the marginal length defined as

$$\ell = -\log_2 p(u|c) \tag{13}$$

where $u$ is the value of the pixel and $c$ is the context. The marginal length is the number of bits needed to compress the current pixel, and is less than 1 when compression is performed. A negative $\Delta L$ value reduces the encoding length of the image and makes this pixel a profitable flip. One way of getting an even higher compression ratio using this loss-introduction algorithm is to pass over the entire image multiple times. Since this increases the execution time for the algorithm and further decreases the quality of the image, it was not considered here.

### 3.2. REGION OF INTEREST PROCESSING

Table 1

Loss introduction parameter values

| parameter | quality | | | |
|---|---|---|---|---|
| | perfect | high | med | low |
| $n_{max}$ | 0 | 2 | 4 | 16 |
| $g_{max}$ | N/A | 0.25 | 2.0 | 16 |
| $s$ | N/A | 0.5 | 0.25 | 0.0 |

Region of interest (ROI) processing allows little or no loss in regions where objects of interest are located. The low-latency greedy flipping utilizing forgetful error diffusion method can be modified to accommodate ROI processing by modifying its parameters as the image is traversed. Four quality levels are defined for this process: perfect (or lossless), high, medium and low. Table 1 shows the parameter values associated with each quality level. The values of $n_{max}$ are always set to even numbers to promote complementary bit flipping. Note that for perfect quality there are no passes through the block. The $g_{max}$ value for high quality was chosen so that two flips could not be done in the same block unless they were opposite flips. The parameters $\tau_\ell$ and $\tau_L$ are set to 1.0 and 0.0 respectively for all quality levels. These parameters were chosen so that any flip that decreases the encoding length of the image can be done if the parameters in Table 1 allow it. Using ROI processing, maximum compression efficiency and visual appearance can be achieved.

## 4. RESULTS

Initial benchmarking compared the BACIC algorithm with G3, G4, JBIG and JBIG2 (Table 2). BACIC performed well compared to these standard methods. Near-lossless compression results were first obtained by introducing constant loss throughout the image, without ROI considerations.

Table 2

Lossless compresion results

| halftoning method | compression ratio for method shown | | | | |
|---|---|---|---|---|---|
| | G3 | G4 | JBIG | JBIG2 | BACIC |
| clustered-dot dither | 0.557 | 0.566 | 3.990 | 4.615 | 4.642 |
| dispersed-dot dither | 0.321 | 0.323 | 3.627 | 4.449 | 4.608 |
| error diffusion | 0.380 | 0.384 | 1.448 | 1.755 | 1.786 |

Table 3

Near-lossless compression ratio results

| halftoning method | quality | | | |
|---|---|---|---|---|
| | perfect | high | med | low |
| clustered-dot dither | 4.642 | 6.024 | 7.570 | 9.526 |
| dispersed-dot dither | 4.608 | 6.267 | 7.595 | 9.440 |
| error diffusion | 1.786 | 1.927 | 2.038 | 2.214 |

Table 3 shows the resulting compression ratios for halftoned images compressed at different quality levels. Figures 2-4 show near-lossless image compression examples at various quality levels. Although loss is noticeable in these images, image quality does not degrade significantly, especially at high quality. As expected, quality is progressively reduced at medium and low quality levels.

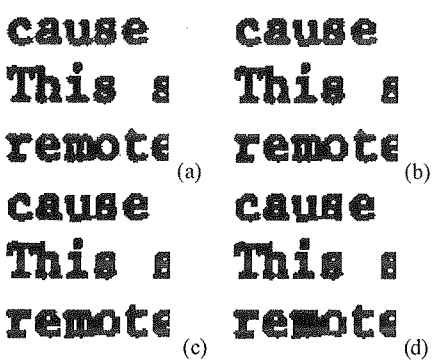


Fig. 2. Near-lossless compression of a document image (a) original; (b) high (c) medium and (d) low quality

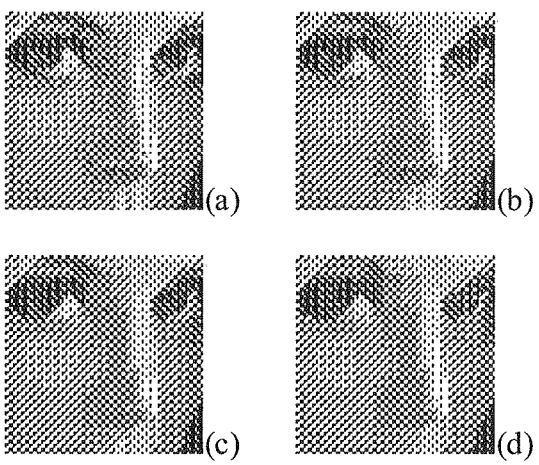


Fig. 3. Near-lossless compression of dithered image (a) original; (b) high (c) medium and (d) low quality

An example of loss introduction with ROI processing is shown in Figure 5. The ROI (face region) was processed at perfect quality and the rest of the image was processed at low quality. Due to ROI processing, the resulting image is acceptable despite the low quality of the background. The overall compression ratio increased over 12% compared to lossless compression. In general, the compression improvement depends on the quality settings, ROI size, image structure and halftoning method used. Using similar settings for a dithered halftone, the increase in the compression ratio over lossless compression was over 40%.

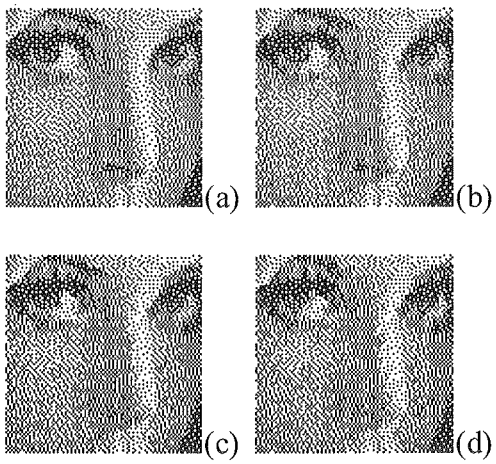


Fig. 4. Near-lossless compression of error diffused image (a) original; (b) high (c) medium (d) low quality

Fig. 5. Lossy cmpression with ROI setting around the facial area; perfect quality inside ROI and low quality elsewhere; CR=2.236 compared to lossless CR=1.990

## 5. FGPA IMPLEMENTATION

The hardware implementation of the lossy to lossless bitonal compression system was performed on a Xilinx XCV-300 Virtex FPGA. The top level design consists of four modules as seen in Figure 6: Memory Controller, Divider, Context Generator and BACIC Encoder/Decoder. The functionality of each of the modules was modeled in Very High Speed Integrated Circuit Hardware Description Language (VHDL).

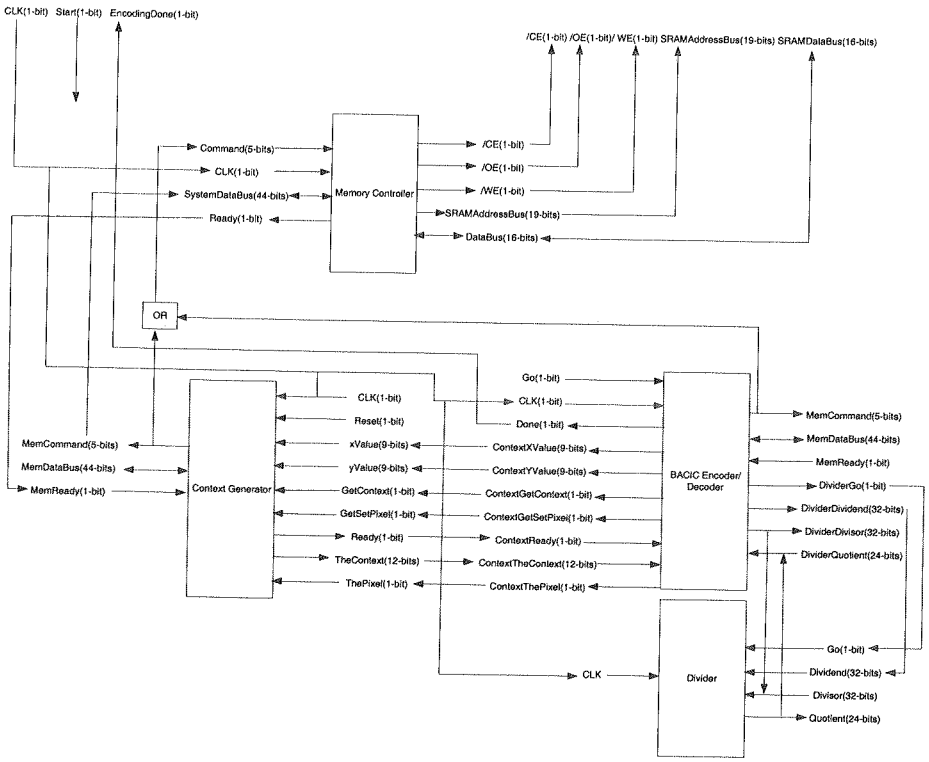


Fig. 6. Top level design

### 5.1. MEMORY CONTROLLER

The Memory Controller provides the interface between external SRAM memory and the compression system. Table 4 shows the controller's custom functions that have been developed to support the needs of the Context Generator and BACIC Encoder/Decoder.. The signals Command, SystemDataBus and Ready connect the Memory Controller with the Context Generator and BACIC modules. The Command is used to tell the memory controller which function to perform. The SystemDataBus is used to pass parameters into the memory controller as well as get return data from the memory controller. The length of 44 bits was chosen to allow for all commands to be done in

parallel. The commands that need the largest parameter and return value size are the GETRI, GETSI, SETRI and SETSI. The GETRI and GETSI both need 12-bits for the context as an input and 32-bits as the return type. The SETRI and SETSI both need 12-bits for the context as an input and 32-bits as the value for an input. The Ready bit is used to tell the component using the Memory Controller that the read or write is finished.

Table 4

Memory controller functions

| function name | function description |
|---|---|
| DONOTHING | used when the memory controller should be idle |
| GETIMAGESIZE | returns the size of the image |
| GETPIXELGROUP | returns a group of 16 pixels to generate the context and get the pixel values |
| GETRI | returns current $r_i$ for a given context |
| GETSI | returns current $s_i$ for a given context |
| GETFUNCTEMPLATE | returns the function (encoding/decoding) and template |
| GETWORD | returns a word from the compressed data memory block |
| SETPIXELGROUP | sets the value of a group of 16-bit pixels |
| SETRI | sets $r_i$ for a given context |
| SETSI | sets $s_i$ for a given context |
| SETWORD | sets a word in the compressed data memory block |
| SETCOMPRESSEDSIZE | sets the word in the compressed size memory block |

### 5.2. DIVIDER

The Divider module is used to calculate the estimated probability $p_1$, as specified in Equation (1). The Dividend and Divisor are the inputs to the divider block and the Quotient is the fractional output. The Go bit is used to start the Divider. Through simulation it was determined that the Quotient needs to be 24 bits in length in order to provide the precision required by the BACIC Encoder/Decoder.

### 5.3. CONTEX GENERATOR

The Context Generator module allows getting the value of the current pixel and its context. It also allows for a set pixel to occur in the case of decoding. The inputs

xValue and yValue provide the location of the current pixel. The GetContext and GetSetPixel inputs tell the module which function to perform. When the GetContext input is asserted, it gets the context for the pixel at the location given by the xValue and yValue parameters. The GetSetPixel is used to either get or set the value of a pixel depending on the operation mode. The Ready output tells when the value of the context or pixel has been returned or the write is complete and is ready for the next command. The output TheContext returns the value of the context upon a GetContext command or returns the value of the pixel, in the lowest bit, for a GetPixel command. The ThePixel input is used for a SetPixel command to specify the value of the pixel.

### 5.4. BACIC ENCODER/DECODER

The BACIC Encoder/Decoder module performs the actual processing of the image data. The Go input starts the processing and the Done output informs when the encoding or decoding is complete. The majority of the functionality for this module is implemented using two Moore state machines, one for encoding and one for decoding. The details of the operations executed during encoding process are shown in Figure 7. The state machine starts in the GETFIRSTCONTEXT state and then goes to the GETFIRSTPIXEL1 and GETFIRSTPIXEL2. These three states together get the first pixel and the first context. No $r_i$ or $s_i$ fetch or division are needed for the encoding of the first pixel as the $p_1$ holds the initial value of 0.5. The get context operation is done due to a requirement of the Context Generator. With the exception of the first pixel, the DISPATCH would be the first state to run. In this state the division is started and while it is occurring, the next context and the next pixel values are found in the states GETNEXTCONTEXT1, GETNEXTCONTEXT2 and GETNEXTPIXEL. After the division is completed the WRITERI1, WRITERI2, WRITESI1, and WRITESI2 states write the $r_i$ and $s_i$ values to the memory. The fetch of the current $r_i$ and $s_i$ values is done next in the GETRI1, GETRI2, GETSI1 and GETSI2 states. The encoding is performed in states ENCODING1 and ENCODING2.

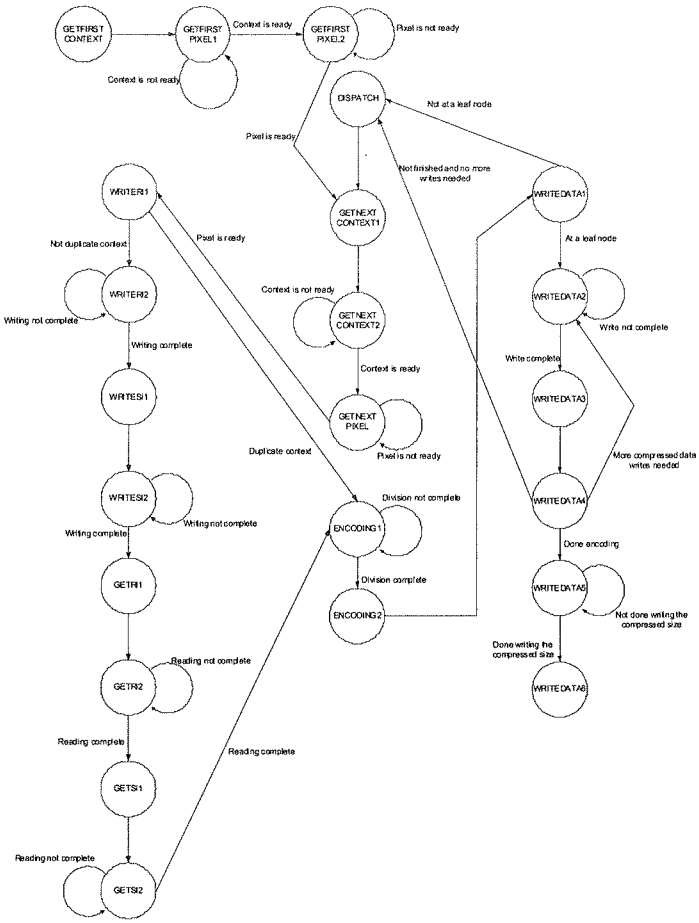


Fig. 7. BACIC encoding state diagram

The WRITEDATA1 state checks to see if memory write is required. If not, the system goes to the DISPATCH state and the process starts all over again. However when the current node value is a 1 or the current pixel is the last pixel in the image, then the state machine visits the WRITEDATA2, WRITEDATA3 and WRITEDATA4 states to write the codeword to the memory. After the entire image has been encoded then the system goes to the WRITEDATA5 state and if the encoding is not completed it goes to the DISPATCH state where the process starts all over. In the WRITEDATA5 and WRITEDATA6 states the compressed size of the image is written and the encoding process is complete.

The operations executed during the decoding process are shown in Figure 8.

The state machine starts by reading the first context, which will always be 0 but is necessary to initialize the context generator. The next state, READDATA1 checks to see if more codewords are needed and if they are, it goes to the READDATA2

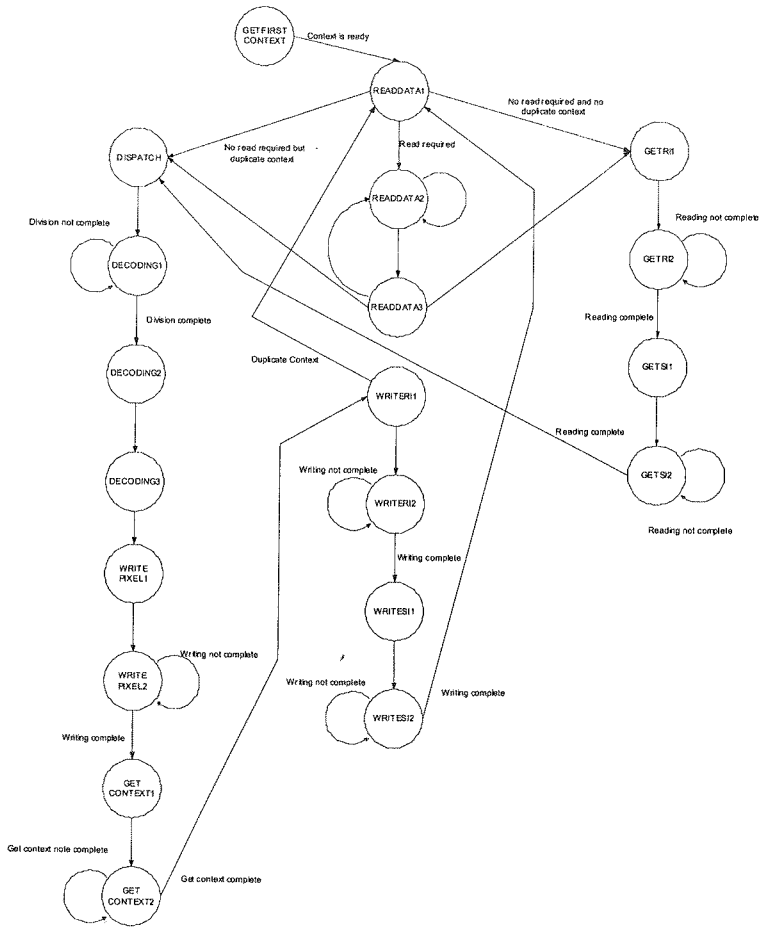


Fig. 8. BACIC decoder state diagram

and READDATA3. The $r_i$ and $s_i$ values are read in the GETRI1, GETRI2, GETSI1 and GETSI2 states. After that the system goes to the DISPATCH state, which starts the division to compute $p_1$. After the division is started, the system goes to state DECODING1 and waits for the result. Once the division is completed, the decoding of the current pixel is done in three steps. After the decoding states have finished, the current pixel value is known as well as the $r_i$ and $s_i$ values to be written. The next step is to get the next context and see if two sequential pixels have the same context. If they do, then the $r_i$ and $s_i$ values are not written for the current pixel or read for the next pixel. If there is not a duplicate context, the system will write the $r_i$ and $s_i$ values in the WRITERI1, WRITERI2, WRITESI1 and WRITESI2 states. The system then returns to the READDATA1 state where the validity of the current codewords is checked and the process starts over again. The design used 92% of the chip area, operated at 41.259 MHz clock frequency, and had power dissipation of 546.61mW. The FGPA hardware

outperformed software implementation in C for both compression and decompression, as shown in Table 5.

Table 5

Hardware performance of FPGA system for bitonal compression system (times are shown in ms)

| image type | Action | SW time | HW time | speedup |
|---|---|---|---|---|
| error diffusion | Compress | 462 | 203 | 2.28 |
| error diffusion | Decompress | 472 | 369 | 1.28 |
| dithered | Compress | 439 | 206 | 2.13 |
| dithered | Decompress | 443 | 371 | 1.19 |

## 6. CONCLUSIONS

This paper presented the FPGA implementation of a lossless to lossy compression system for bitonal images that maximizes compression efficiency and visual quality. The system can adjust loss introduction according to quality settings and ROI processing. The FPGA hardware implementation outperformed software for both compression and decompression.

## 7. ACKNOWLEGMENTS

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# Hardware architecture of a parallel system for lane detection

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The aim of this paper is to describe in detail the hardware implementation of the lane detection algorithm presented at 15th International Conference "Mixed Design of Integrated Circuits and Systems". During introductory research several approaches to edge and line detection were analyzed, which resulted in optimal combination for future hardware implementation. The proposed algorithm is based on the Canny edge detector and the linear Hough transform for line detection. The system was pre-developed using the Matlab environment. The next step was the synthesizable hardware description using VHDL. A wide range of testing procedures for structural and behavioral verification was designed. The presented evaluation of both hardware and software simulation, and synthesis results suggested high capabilities of designed architecture, which have been proven during real-time hardware tests of the system.

*Keywords:* Lane detection, VHDL, Canny edge detection, hough transform FPGA

## 1. INTRODUCTION

Image processing finds more and more applications nowadays. In particular it is becoming widely used in autonomous vehicle control tasks, where vision-based systems have been proven to be superior to other methods of environment navigation. For real-time image processing, in most cases the implementation of a parallel algorithm is necessary. Parallel implementations are usually based on either a multiprocessor computer or on computer clusters. However clusters of computers or multiprocessor computers itself are not feasible solution in all situations, because of high power consumption, size or cost. In such cases a dedicated solution based on FPGA or ASIC is a competitive proposal.

In this paper we present a parallel architecture for a complete vision-based lane detection system implemented in VHDL. The proposed algorithm is based on [5] and consists of two stages: Canny edge detection [4] and linear Hough transform [1] for line detection. Having information from these two steps we can calculate the essential parameters of the road, including the left and right lane and the mid-line of road.

## 2. THEORY

### 2.1. THEORETICAL ASPECTS OF VISION-BASED LANE DETECTION SYSTEMS

The most common technique used for a first step of digital image processing is edge detection. Almost every shape can be described using only its boundaries. If we can detect edges well enough we will be able to isolate certain items of interest to further analysis, which is the main idea of image processing.
Before presenting the methodology of edge detection, the idea of an Ideal Step Edge should be explained. It means monochromatic luminance change along the some arbitrary curve. The more rapid the transition, the easier it is to identify an edge. Figs. 1 and 2 show the plot of luminance change for a particular row in an image.

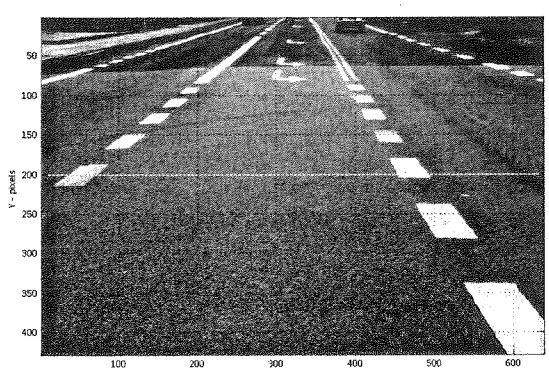


Fig. 1. Luminance change plot for row y=200 in the image

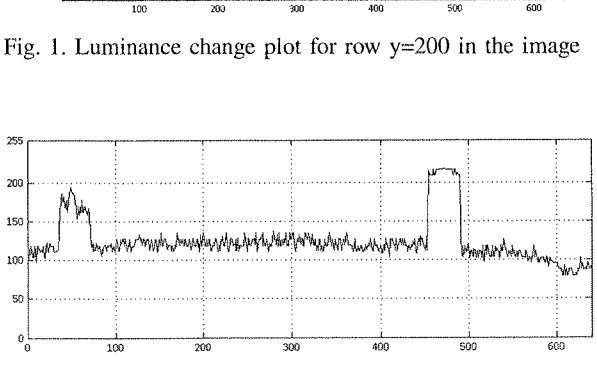


Fig. 2. Luminance change plot for row y=200 in the image

The main problem for any video processing algorithm is Signal-to-Noise-Ration (SNR) of input data, as every analog-to-digital conversion always results in noise in analyzed data. Due to that fact many different edge detection techniques have been developed, from very simple solutions to more sophisticated ones. Fig. 3 presents an example of noise and quantization error in photography of the road.

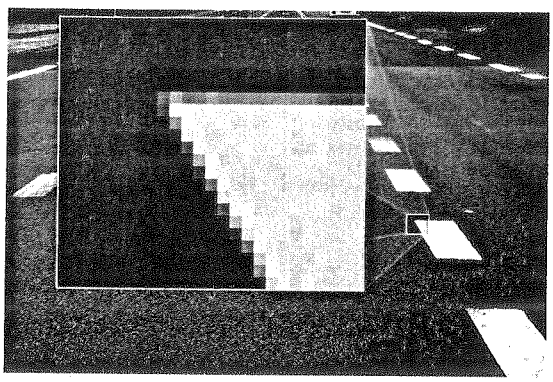

Fig. 3. Example of noise distorion and quantization error in road image

In choosing the right edge extraction technique for particular application, it is important to remember that every edge detector should detect all the edges from the image, at the same time avoiding false detection. The distance between isolated edge pixels and "real" edge pixels should be minimal. Moreover the edge detection should result in one-pixel width edges. Keeping all that in mind, we should choose an algorithm that combines optimal result and performance for the particular system.

### 2.2. CANNY EDGE DETECTION

In order to detect road lanes we must use some image segmentation techniques, such as edge and line detection. We have chosen the Canny edge detector for the first stage of analysis. This operator is based on gradient calculations to enhance edges, hence it can be easily implemented in the FPGA structure using 2D convolution combined with the moving window architecture [4]. The following steps that need to be taken to implement the Canny edge detector. First, in order to suppress any possible noise in the image, the input data is smoothed by Gaussian convolution (whose mask is estimated using Equation 1).

$$G_\sigma(x,y) = \frac{1}{2\pi\sigma^2} e \frac{-(x^2+y^2)}{2\sigma^2} \tag{1}$$

Next, in order to obtain gradient information we must compute the image derivatives in both directions. In FPGA implementation these derivatives can be approximated by Prewitt operators presented in Figure 4. After performing gradient calculations for an image, the magnitude or, edge strength has to be calculated. The function of the third

step, known as non-maximum suppression, is to find edge points which are assumed to be gradient magnitude local maxima in the gradient direction. We can achieve this by suppressing all pixels whose intensity is not maximal within a certain neighborhood. Using simple interpolation of the surrounding discrete grid values in proper direction, we can compare interpolated values to a gradient magnitude of a considered pixel. If a pixel value is not greater than these values it is suppressed. Figure 5 and Table 1 explain the idea further.

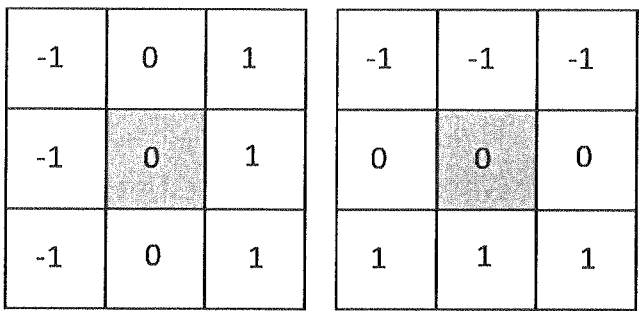


Fig. 4. Example Prewitt operators

Hysteresis thresholding [2], the last step of the Canny edge detector uses high and low thresholds to finally determine which pixels can be marked as an edge. If the pixel value is greater than $T_h$(high threshold) it is classified as an edge and every pixel with value between $T_h$ and $T_l$ (low threshold) that is in close neighborhood of it is considered also as an edge pixel. If the pixel value is within the range $T_h$ and $T_l$ but there is no "edge" pixel in given neighborhood, the considered pixel is marked as non-edge the same as pixels with the value below low threshold.

Table 1

Interpolation equations

| Angle ranges | Interpolation equations |
|---|---|
| 0°-45° | $P_A = \frac{P_{(x+1,y+1)} + P_{(x+1,y)}}{2}, P_B = \frac{P_{(x-1,y-1)} + P_{(x-1,y)}}{2}$ |
| 45°-90° | $P_A = \frac{P_{(xy+1)} + P_{(x+1,y+1)}}{2}, P_B = \frac{P_{(x-1,y-1)} + P_{(x,y-1)}}{2}$ |
| 90°-135° | $P_A = \frac{P_{(x,y+1)} + P_{(x+1,y+1)}}{2}, P_B = \frac{P_{(x-1,y-1)} + P_{(x,y-1)}}{2}$ |
| 135°-180° | $P_A = \frac{P_{(x-1,y)} + P_{(x-1,y+1)}}{2}, P_B = \frac{P_{(x+1,y-1)} + P_{(x+1,y)}}{2}$ |

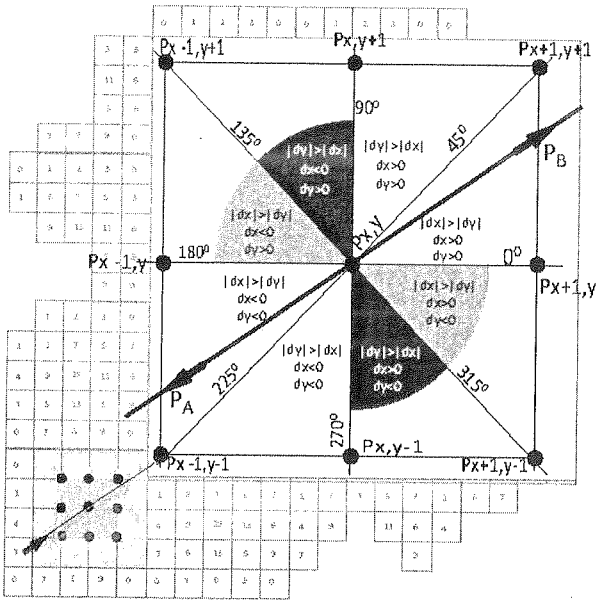


Fig. 5. Non-maximal suppression scheme

### 2.3. HOUGH TRANSFORM

The second stage of the analysis consists of the linear Hough transform for straight-line detection. We can analytically describe a line in a number of forms. However, a convenient equation for describing a set of lines uses parametric notation (Equation 2), where parameter r represents the distance between the line and the origin, while θ is the angle of the vector from the origin to this closest point.

$$r = x \cdot \cos\varphi + y \cdot \sin\varphi \tag{2}$$

Each point $(x_i, y_i)$ of the earlier detected edges is transformed into a sinusoidal curve and accumulated in the (r, θ) space, also called Hough space or the accumulator. An example of this operation presented in Figure [6]. The resulting peaks in the accumulator are strong evidence that a corresponding straight line exists in the image. The Figure [7] presents an example of accumulator for a single straight line in an image.

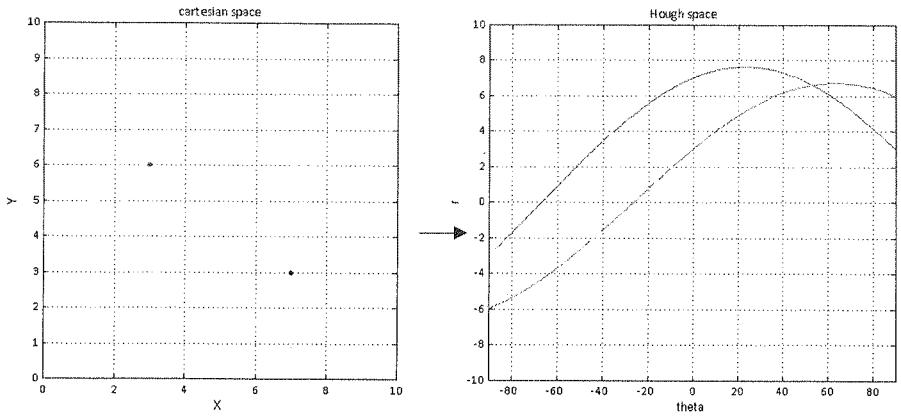


Fig. 6. Example transformation of two separate points into Hough space

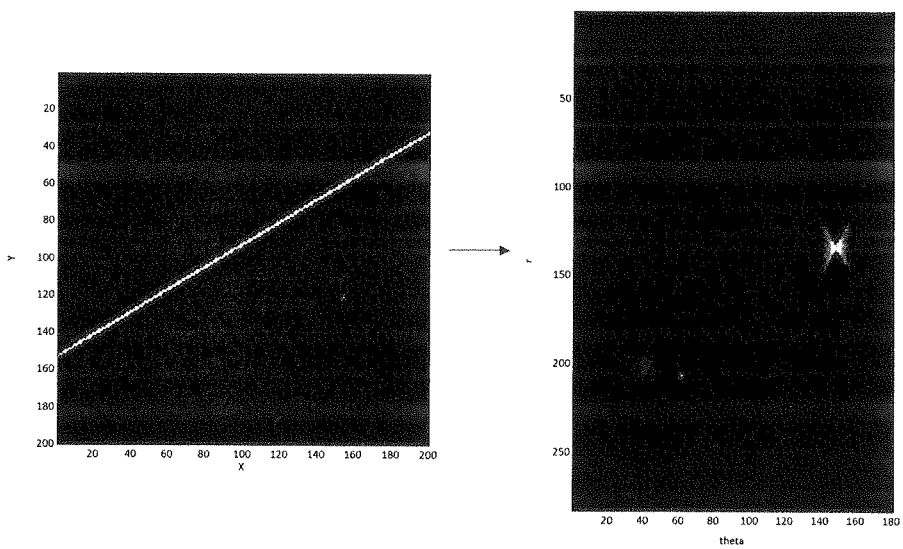


Fig. 7. Example Hough space for a single straight line

Given line parameters of extracted with Hough transform right and left lanes of road, we can easily estimate the road mid-line parameters with equations 3-10 (compare line segment CD in figure 8).

$$y_A = \frac{y}{2} \tag{3}$$

$$x_A = \frac{r_2 + y_A \sin\theta_2}{\cos\theta_2} + \frac{x}{2} \tag{4}$$

$$y_B = \frac{y}{2} \tag{5}$$

$$x_B = \frac{r_1 + y_b \sin\theta_2}{\cos\theta_2} + \frac{x}{2} \tag{6}$$

$$y_C = \frac{r_2 \cos\theta_2 + r_1 \cos\theta_2}{\sin(\theta_2 - \theta_1)} + \frac{y}{2} \tag{7}$$

$$x_C = \frac{r_2 \sin\theta_1 + r_1 \sin\theta_2}{\sin(\theta_1 - \theta_2)} + \frac{x}{2} \tag{8}$$

$$y_D = \frac{y}{2} \tag{9}$$

$$x_D = \frac{x_A + x_B}{2} \tag{10}$$

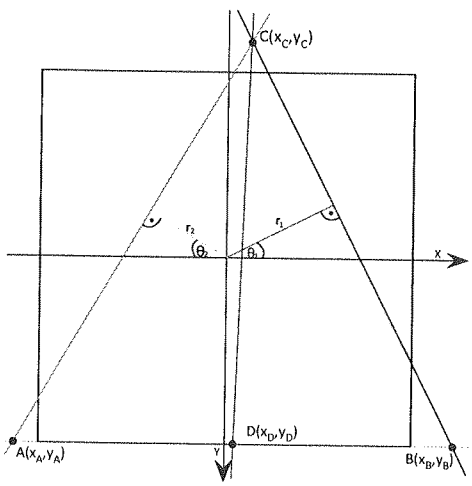


Fig. 8. Example of mid-line parameters extraction

## 3. ARCHITECTURE

As mentioned before, a video-based autonomous vehicle solution capable of performing real-time analysis requires a parallel processing system, either a multiprocessor computer, a computer cluster or an appropriate parallel design dedicated for either a FPGA or ASIC. Since our vehicle model had some limitations not only in terms of space availability, the chosen solution was to design a highly parallel pipelined architecture dedicated for a FPGA core. The main objective was to develop the system able to produce a new result with every rising clock edge of a system clock, without any delay. To accomplish this task we designed a complex structure based on cascaded

FIFO queues. In order to acquire a fully scalable architecture each FIFO was implemented using Block RAM [6] embedded in target device. Thanks to the proposed structure we achieved the moving window architecture that implemented all our initial requirements. Having the core of the proposed system, our next aim was to implement both the Canny edge detection algorithm and the Hough transform, in a synthesizable form for the FPGA platform.

## 3.1. CANNY EDGE DETECTION

### *3.1.1. GAUSSIAN BLUR MODULE*

As described in the Theory section of this paper, the first step of Canny edge detection is filtering out the noise from the image, using Gaussian blur operation. The implementation based on FPGA requires designing a module capable of calculating a 2D discrete convolution with a fixed-point value mask. For the discussed system we chose a 5-by-5 mask pre-calculated in our Matlab implementation. Unfortunately, the coefficients of Gaussian mask are real numbers in the range $< 0; 1 >$ which cannot be represented in the synthesizable syntax of VHDL does. Therefore we chose to use the fixed-point arithmetic, and the IEEE-proposed package for VHDL [2] implementing both fraction representation and all necessary arithmetic operations in a digital circuit. For our design we chose a representation with total word length ten bits (one sign-bit and nine fraction bits). The results for the mask, calculated with both floating and fixed-point precision, are given in Figs. 9 and 10.

| | | | | |
|---|---|---|---|---|
| 0.0005 | 0.0050 | 0.0109 | 0.0050 | 0.0005 |
| 0.0050 | 0.0521 | 0.1139 | 0.0521 | 0.0050 |
| 0.0109 | 0.1139 | 0.2487 | 0.1139 | 0.0109 |
| 0.0050 | 0.0521 | 0.1139 | 0.0521 | 0.0050 |
| 0.0005 | 0.0050 | 0.0109 | 0.0050 | 0.0005 |

Fig. 9. Used Gaussian mask, floating-point precision

| | | | | |
|---|---|---|---|---|
| 0.0000 | 0.0059 | 0.0117 | 0.0059 | 0.0005 |
| 0.0059 | 0.0527 | 0.1133 | 0.0527 | 0.0059 |
| 0.0117 | 0.1133 | 0.2480 | 0.1139 | 0.0117 |
| 0.0059 | 0.0527 | 0.1133 | 0.0527 | 0.0059 |
| 0.0000 | 0.0059 | 0.0117 | 0.0059 | 0.0005 |

Fig. 10. Used Gaussian mask, fixed-point precision

The shown difference in coefficients was acceptable in terms of noise filtering, and fixed-point mask was implemented as a Look-Up-Table for calculation. In Gaussian blur module we introduced buffering method similar to the method used in the moving window architecture. In this way we accomplished a fully parallel synthesizable design of a video noise reduction module capable of producing a result without any delays.

### *3.1.2. DERIVATIVE CALCULATIONS MODULE*

The second step consists in calculating the derivatives of the image in both horizontal and vertical direction. As described earlier in hardware implementation we used the Prewitt operators which are based, similarly to our Gaussian blur module, on 2D digital convolution, but since the masks used here have integer coefficients, the implementation was much easier then previous module.

### *3.1.3. NON-MAXIMAL SUPPRESSION MODULE*

Non-maximal suppression is the next step of Canny edge detection. The algorithm of this module was presented earlier in Theory section. First the values of two derivatives are combined together using the taxicab norm. Originally instead of taxicab norm, Euclidian norm was used. However this approximation simplifies implementation, without significant influence to the results. After having calculated the gradient we can suppress false maxima from the created data. Since we need to know the values of surrounding pixels we created another cascaded buffer inside the module, quite similar to buffers used in Gaussian blur and derivative modules. The equations were directly inherited from the Matlab implementation. Again, using the moving window architecture we have managed to parallelize another step of the Canny edge detector.

### *3.1.4. HYSTERESIS THRESHOLDING MODULE*

Final step of the Canny edge detector is hysteresis thresholding. Basing on neighborhood of analyzed pixel we can determine whether this pixel can be classified as an edge pixel or not. The result yielded by this particular module is a one-bit value, where logical "1" corresponds to an edge pixel and "0" to a non-edge pixel.
Example results of the RTL code simulation for Canny edge detector are presented in Figs. 11 and 12.

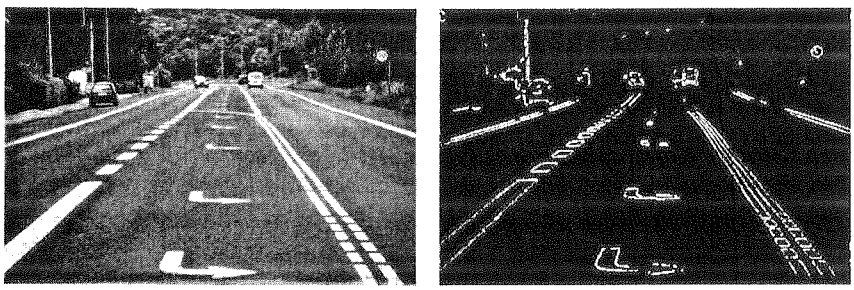

Fig. 11. Implemented Canny edge Detector

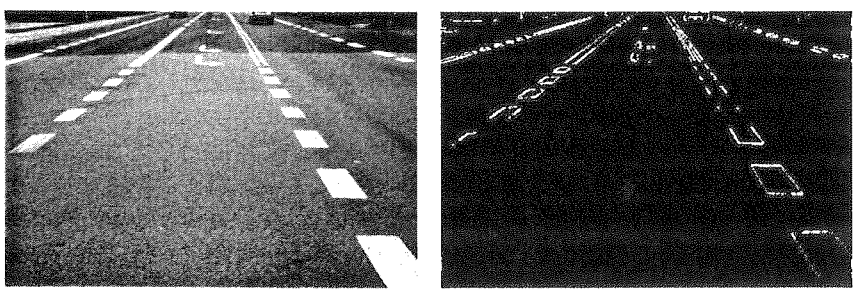

Fig. 12. Implemented Canny edge detector

## 3.2. HOUGH TRANSFORM MODULE

The second part of the system consists of isolating straight lines from the image. Having information about all existing edges in the data stream, we can calculate the r and θ parameters of each possible line with the parametric Equation 1 describing Hough transform. The module processes data, giving results for $\theta\epsilon$ (-90°;90°) with 3° step, which gives us sixty 10-bit r values corresponding to sixty values of parameter θ. Calculations of sine and cosine functions were implemented using Look-Up-Tables.

The original design implied building a Hough space using a serial algorithm. Therefore, we intended to implement this particular function in an embedded PowerPC core. The architecture of this design is presented in Figure 13.

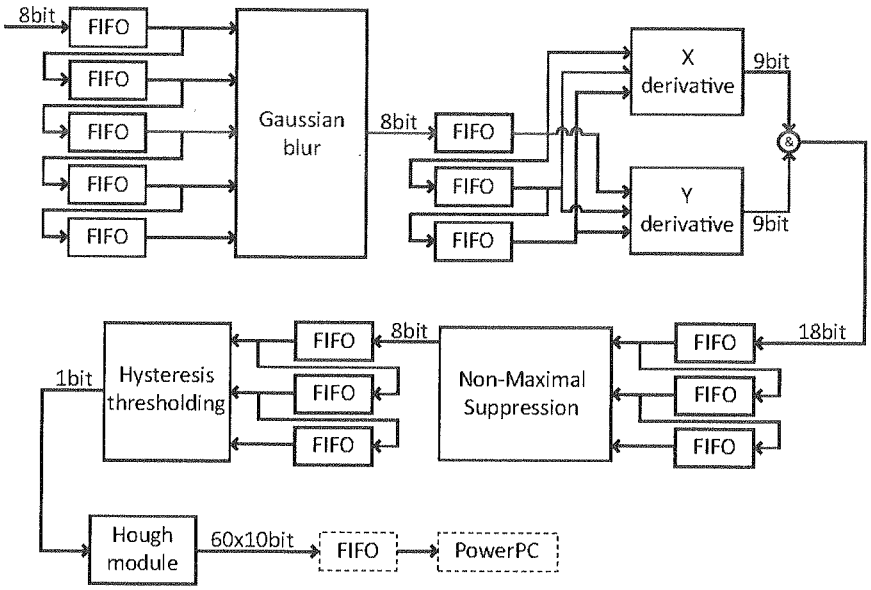


Fig. 13. Original architecture of the system

However, recently we have managed to parallelize the process of creating the accumulator and create a synthesizable VHDL code describing the appropriate module. The basic idea is to use sixty BlockRAMs. In each memory block we increment the value of the cell, whose address is given by the calculated value r. In this way we can increment sixty values at once, still having a fully pipelined system.

Building the Hough space is not only part of the serial algorithm mentioned before. The second part is isolating two most dominant pairs of values (θ, r) corresponding to two lines in the image. Since we already had a parallelized accumulator, we have created an additional module, an instance of which is connected to each BlockRAM (60 modules total), that stores the maximum value and the address of the corresponding memory cell. Each time a new set of parameters r is calculated, the module compares the value it currently stores with the new incremented one. If the new value is greater, then it is stored together with the address of a particular memory cell with the new maximum. In this way we have the maximum value in each BlockRAM. The outcome of each module is compared with outcomes of other modules, resulting in two pairs of values (θ, r) corresponding to two lines we are looking for. The modified version of the system is presented in Figure 14.

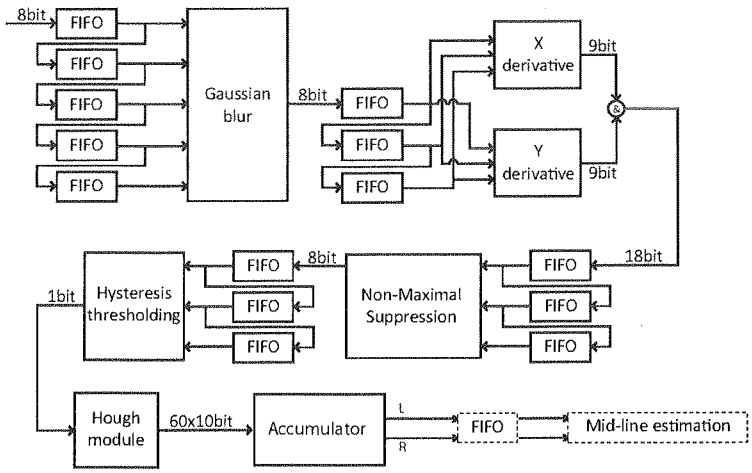


Fig. 14. Modified architecture of the system

Example Matlab simulation results of the Hough Transform are presented in Figs. 15 and 16.

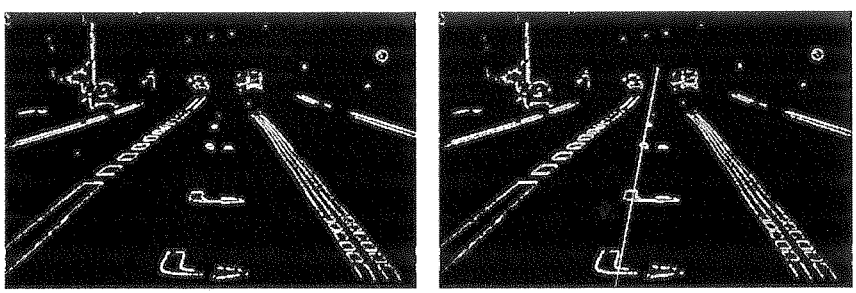

Fig. 15. Matlab result of road mid-line estimation

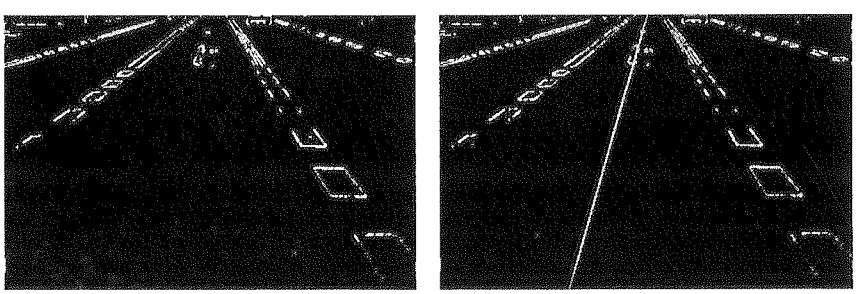

Fig. 16. Matlab result of road mid-line estimation

## 4. REAL TIME VERIFICATION

After extensive software-based verification executed in Mentor Modelsim testing environment we have decided to prove real-time capabilities of the designed architecture by testing it in FPGA device. Therefore we have developed hardware processing unit to adapt video signal from Analog's Devices ADV7183B 24-bit A/D converter to our needs. In default configuration output of device mentioned above is compliant to ITU-R Recommendation BT.601 (YUV 4:2:2), while our system requires input in RGB standard.

Also due to limited memory resources on our testing platform (Digilent Inc. Virtex II-Pro Development Board – presented in figure 17) it was necessary to avoid buffering input video signal. Input data is received from Digilent Inc. Video Decoder (figure 18) then processed and directly displayed on a VGA compliant device. At MIXDES 2008 conference we demonstrated real-time processing of the video signal obtained from the camera mounted on a car.

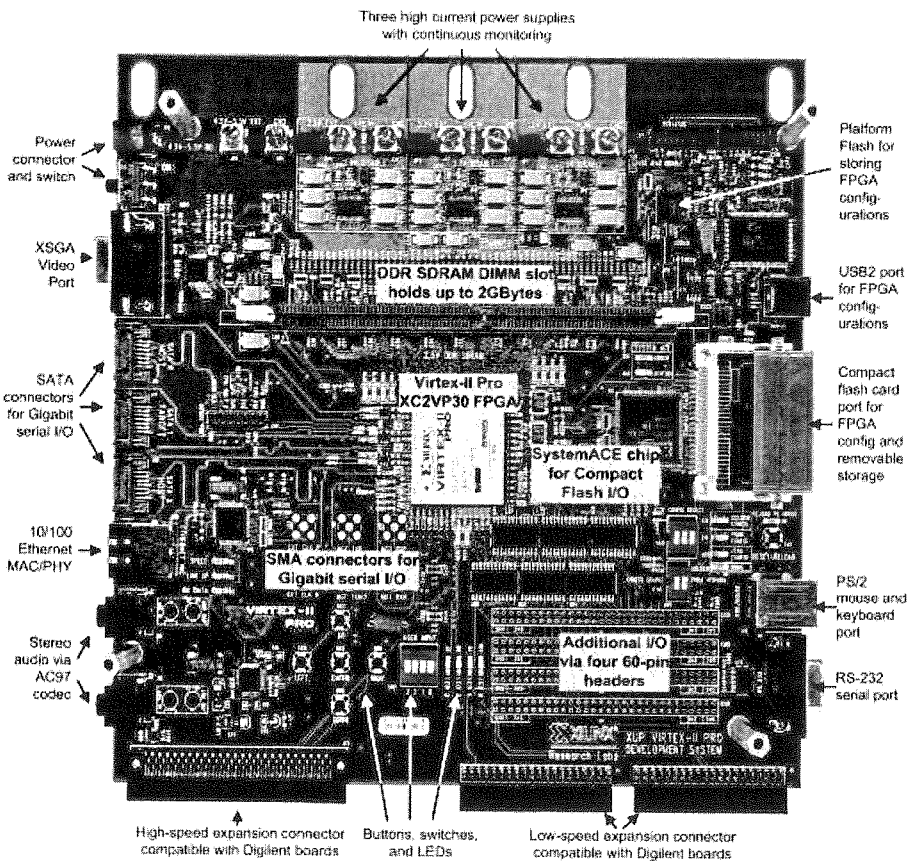


Fig. 17. Testing platrform (XUP-V2P

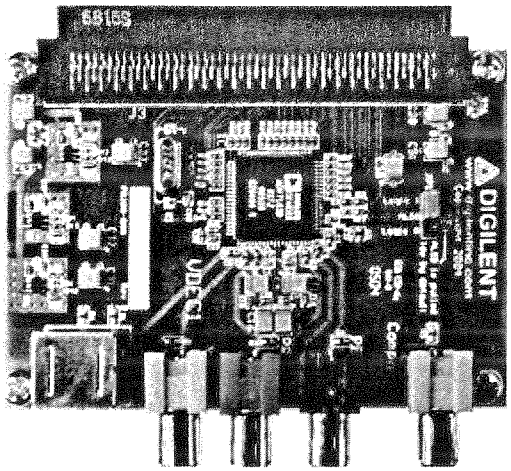


Fig. 18. Digilent Inc. Video Decoder Board

## 5. CONCLUSION

In order to develop a vision-based lane detection system, a highly-parallel pipelined architecture was proposed. Simulations and hardware verification proves that the presented solution is suitable for real-time video analysis. The design was developed in a modular way which makes future modifications possible to implement.

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# Numerical aspects of multiple-sensor measurements with potentiometric sensors

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The paper compares accuracy and measurement range for two techniques of multiple-sensor measurement of ion concentration in water with potentiometric ion selective sensors: a single-sensor-at-a-time measurement and multi-sensor Data Fusion based measurement. A problem of entangled measurement ranges is defined and a rational solution presented.

*Keywords:* calibration-based measurement, measurement uncertainty, potentiometric sensors, Nikolsky-Eisenmann model, non-linear least squares model fitting

## 1. INTRODUCTION

Data processing of raw measurements is commonly used to provide requested accuracy, precision and measurement range of measurement instruments, despite limiting non-ideal properties of sensors used – such as nonlinearity, drift of sensor responses and ageing. For chemical sensors, such as potentiometric ones [1,2] (to be considered here) there is a need for compensation of other, chemistry specific effects: finite sensor selectivity towards interfering ions ("matrix effect"), dependence of quasi-linear measurement range on activity of interfering ions, indirect influence of sensor responses by ionic strength of the water sample. This paper presents the problem of activity estimation of selected ions in clean water from the mathematical/metrological perspectives. Two measurement techniques will be formulated – a basic (single-sensor-at-a-time) Pre-Calibration based Measurement (PCM) and its multi-sensor extension, based on Data Fusion (DF) concept [3]. The paper presents some new information on systematic

inaccuracy of the two approaches. The work reported here is a part of the author's research activity in the EU FP6 Water Risk Management in EuRope (WARMER) project [4], which intends to create a Web enabled water quality monitoring network, integrating modular multi-sensor in-situ probes and satellite remote sensing – in response to the EU Water Framework Directive [5] request.

## 2. PRECALIBRATION BASED MEASUREMENT (PCM)

For potentiometric sensors, which are considered in this paper, dependence of its steady-state voltage on activity of ions that are present in the water sample, can be approximately described with the classic Nikolsky-Eisenmann (NE) model[1] [6]:

$$U = U_0 + \frac{S}{z_m} \cdot \lg\left(\sum_{j=1}^{I} K_{m,j} \cdot a_j^{z_m/z_j}\right), \quad \text{where} \quad K_{m,m} = 1 \tag{1}$$

$a_m$, $z_m$ denote molar activity and charge number of the main ion (the sensor is most sensitive to), while $a_j$, $z_J$, $j \neq m$ denote activities and charge numbers of the remaining (interfering) ions of the same charge sign. Selectivity coefficients $K_{m,j}$ quantify interfering influence of the $j$-th ion onto the sensor response (the smaller the better). $U_0$ denotes an ion-independent offset voltage, while the slope parameter $S = \ln(10) \cdot V_T$, where $V_T = kT/q = RT/F$ is the familiar electro-thermal potential [7].

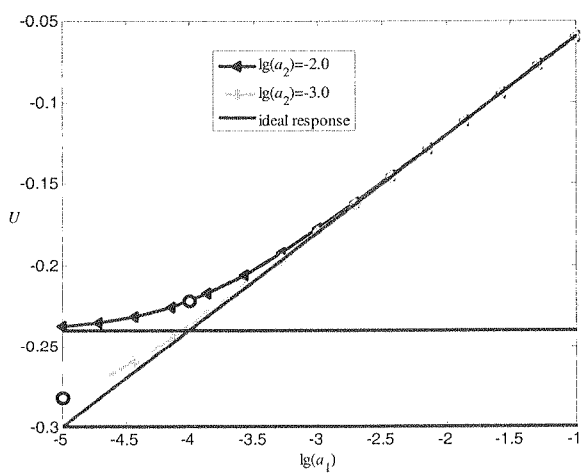


Fig. 1. Example response function of a potentiometric sensor (with selectivity $K_{1,2}$=0.001) for two activity levels of an interfering ion. The circles mark Limit of Detection (LOD) points [7]

[1] There are models, which describe sensor behaviour more accurately, especially for mixtures of ions with different ion charges [8,9]. However, the NE model represents sensors sufficiently well to expose fundamental difference between presented approaches to ion measurement.

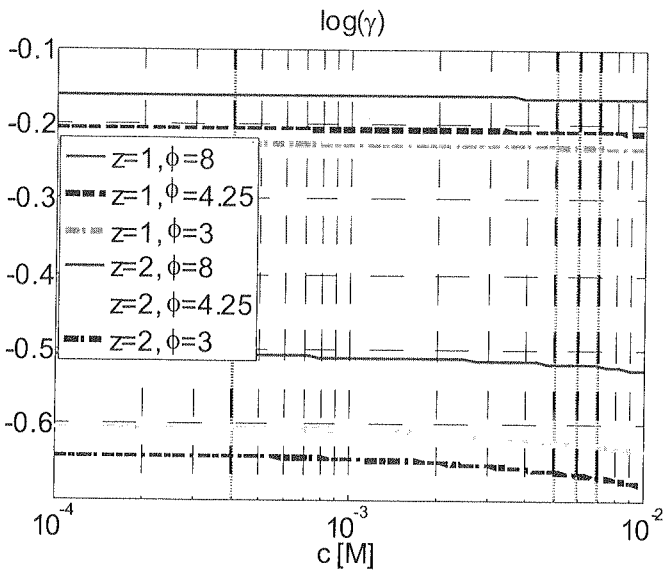


Fig. 2. Example dependence of activity coefficient on ionic concentration $c$, charge number $z$ and effective ion diameter $\phi$, for 0.1M lithium acetate ISAB

It is seen from equation (1) and its example visualisation in Fig. 1 that dependence of sensor response on logarithm of ion activity is pretty linear for activity level at least a decade higher from the "knee-point" abscissa located at the value:

$$\breve{a}_m = \sum_{j=1, j\neq m}^{I} K_{m,j} a_j^{z_m/z_j} \tag{2}$$

which is apropriately called a Lower Detection Limit (LOD) [7] – as it vaguely determines the lower measurement range for single sensor measurement.
Users of chemical sensors are usually not that interested in ion molar activity $a_j$ as they are in molar concentration $c_j$ of each ion. Relationship between the two notions has a deceivingly simple form:

$$a_j = c_j \cdot \gamma_j \tag{3}$$

Unfortunately, the activity coefficient $\gamma_j$ in (3) depends on concentrations $c_i$ and charge numbers $z_i$ of *all ions* in the solution, via so called ionic strength $J$ [7]:

$$\log(\gamma_j) = z_j^2 \frac{A\sqrt{J}}{1 + B\phi_j\sqrt{J}}, \qquad J = \frac{1}{2}\sum c_i z_i^2 \tag{4}$$

A, B coefficients in the Debye-Hückel formula (4) denote some temperature dependent constants, while $\phi_j$ stands for effective diameter of the $j$-th ion. As the Fig. 2 shows the

activity coefficients can be much different for different ions of the same water sample. To reduce measurement uncertainty due to changing ionic strength of the sample (which might be due to concentration variations of ions, which do not influence the sensor response directly) – chemists add some concentrated solution called Ionic Strength Adjustment Buffer (ISAB) to the sample. ISAB does not chemically affect sensors, but makes the activity coefficients constant – as seen in Fig. 2. In what follows we assume, that activity coefficients are made constant by suitable addition of ISAB to all liquids used (including the sample). Necessary dilution of the liquids with ISAB is assumed to occur prior to the measurement, and so the formulae to follow do not contain other terms related to ISAB than activity coefficients.

### 2.1. THE BASIC PCM MEASUREMENT METHOD

For sufficiently high concentration of the main ion the nonlinear NE model (1) simplifies to the following Nernst model, which is linear w.r.t. the frequently used logarithmic measure of ion concentration $p_m = \lg(c_m)$:

$$U = U_0 + \frac{S}{z_m} \cdot \lg(a_m) = \breve{U}_0 + \frac{S}{z_m} \cdot p_m, \quad \text{where} \quad \breve{U}_0 = U_0 + \frac{S}{z_m} \lg(\gamma_m) \tag{5}$$

Having the sensor calibrated prior to actual sensor contact with a water sample under test – the main ion estimate can be calculated by inversion of the model w.r.t. $a_m$, or if the activity coefficient is known – also w.r.t. $c_m$ or $p_m$. Such a measurement procedure, called basic Pre-Calibration Measurement (PCM) technique, will be a reference technique for this paper.

Unfortunately, when the simple model (5) is not sufficient, because of non-negligible interferences – application of the same basic PCM technique complicates. If e.g. NE has to be used – it is still possible to find a function, which inverts relationship $a_m \rightarrow U$ of the following form:

$$a_m = v_m - \sum_{j=1, j\neq m}^{I} K_{m,j} \cdot a_j^{z_m/z_j}, \quad \text{where} \quad v_m = 10^{\frac{z_m}{S}(U-U_0)} \tag{6}$$

Unfortunately the above function is in fact dependent on activities of interfering ions, which are not determined in the basic PCM – and so their variability creates additional measurement uncertainty. The basic PCM technique does not use information on interfering ions and so estimates activity of the main ion as follows:

$$\widehat{a}_m = 10^{v_m} \quad \text{or otherwise} \quad \lg(\widehat{a}_m) = v_m \tag{7}$$

The relative inaccuracy of the basic PCM technique (bias of $a_m$ estimate), which is a measure of this uncertainty, can be expressed as [11]:

$$\delta^{(1)}(a_m) = \frac{\widehat{a}_m - a_m}{a_m} = \frac{\sum_{j=1, j\neq m}^{I} K_{m,j} \cdot a_j^{z_m/z_j}}{a_m} \tag{8}$$

From (2) and (8) one can see, that at the LOD point the inaccuracy of activity estimate is 100%, which is too large for water monitoring applications (which typically require 10% to 20%). The author proposed in [11] a Data Fusion approach to reduce inaccuracy in such measurement situations. The main idea has the following components.

- Instead of one sensor sensitive to the ion of interest – many sensors are used, sensitive also to (at least major) interfering ions.
- All the sensors are calibrated such as to determine relevant selectivity coefficients of each sensor.
- All the sensors are exposed to the same set of liquids (including the sample).
- Read-out data from all sensors are merged (fused) so as to get estimates of the ion of interest with smaller inaccuracy.

Initially the approach was introduced for a multi-sensor generalization of the basic PCM technique (see the following subsection), but was later developed using other measurement protocols, notably the Standard Addition Measurement (SAM) (see e.g. [4,12]). In this paper only the PCM technique will be discussed.

### 2.2. DATA FUSION BASED PCM

Pre-Calibration Measurement (PCM) is a two-phase procedure. The first phase calibrates sensor models, while the second phase interprets sensor read-out with the calibrated model. The basic measurement procedure, detailed in Sec. 2.1, uses a single sensor (at a time). In this section its generalization is introduced that is able to measure jointly (as opposed to one-sensor-a-time) with $M \geq 1$ sensors. Such a multi-sensor measurement technique will be called Data Fusion based PCM, or DF-PCM for short.

The PCM procedure assumes availability of a parametric model of each sensor:

$$U^{(m)} \cong g_m(\mathbf{a}, \mathbf{b}^{(m)}) \tag{9}$$

For our sensors $U^{(m)}$ denotes steady-state voltage response of the $m$-th sensor, after exposition to a solution (sample or standard liquid) with ion activities given by the I-element vector $\mathbf{a}$.

The first phase of DF-PCM requires $K$ expositions of the sensors to different standard liquids; each time a complete set of sensor read-outs is obtained: $\hat{U}^{(k,1)},...,\hat{U}^{(k,M)}$, $k = 1,...,K$. Concentration of ions in the standard liquids will be denoted with a set of I-element vectors $\mathbf{s}^{(1)},...,\mathbf{s}^{(K)}$. Thus the vector of model parameters $\mathbf{b}^{(m)}$ for the $m$-th sensor can be determined by least squares model fitting (optimization):

$$\min_{\mathbf{b}} \left\{ (\mathbf{b}) F_m^{(cal)}(\mathbf{b}) = \sum_{k=1}^{K} \left( w_{m,k}^{(cal)} r_{m,k}^{(cal)}(\mathbf{s}^{(k)}, \mathbf{b}) \right)^2 \right\}, \quad r_{m,k}^{(cal)}(\mathbf{a}, \mathbf{b}) = \tilde{g}_m(\mathbf{a}, \mathbf{b}) - \hat{U}^{(k,m)} \tag{10}$$

Weighting coefficients $w_{m,k}^{(cal)}$ can be used to emphasise measurement data with small uncertainty. If inaccuracy of calibration measurements $\hat{U}^{(k,m)}$ can be represented as independent Gaussian random numbers with 0 mean and standard deviations $\sigma_{k,m}$, than $w_{m,k}^{(cal)} = 1/\sigma_{k,m}$ give estimate of $\mathbf{b}$ with lowest dispersion. Let us note, that for models that are linear w.r.t. $\mathbf{b}$ (e.g. (5)) we have in (10) a linear least squares problem, for which extremely efficient algorithms exist. Unfortunately it is not the case even for NE (1) and not to mention more complicated models [8,9].

The second part of DF-PCM procedure requires that all sensors are exposed to the water sample under tests (with unknown activities $\mathbf{a}$ of the ions of interest) and read-outs $U^{(m)}$ of each sensor are taken. For sufficient number of sensors sensitive to all $I$ ions it is principally possible to evaluate estimates $\tilde{\mathbf{a}}$ of the ion content in the sample by inverting the sensor models – solving e.g. the following optimization problem:

$$\min_{\mathbf{a}} \left\{ F_m^{(mes)}(\mathbf{a}) = \sum_{m=1}^{M} \left( w_m^{(mes)} \cdot r_m^{(mes)}(\mathbf{a}, \hat{\mathbf{b}}^{(m)}) \right)^2 \right\}, \quad r_m^{(mes)}(\mathbf{a}, \mathbf{b}) = \tilde{g}_m(\mathbf{a}, \mathbf{b}) - U^{(m)} \tag{11}$$

As formerly, weighting coefficients $w_m^{(cal)}$ can be used to emphasise measurement data with small uncertainty. In chemical measurement practice it is realistic to expect estimation of only a small subset of ions that can potentially be present in water. It means, that the optimization problem (11) is solved w.r.t. the subset of the whole vector $\mathbf{a}$. Remaining ions parametrize thus obtained solution, and so they are a source of measurement uncertainty. Quantification of that uncertainty is presented next.

### 2.3. ACCURACY OF SINGLE AND MULTI-SENSOR PCM TECHNIQUES

Let us compare inaccuracy of the single and multi-sensor PCM techniques caused solely by presence of interfering ions in the water under test. Inaccuracy of models and optimization algorithms as well as read-out inaccuracy will be assumed negligible.

To simplify presentation let us re-order the vector $\mathbf{a}$ of all $I$ ion activities, so as to create two sub-vectors. The first $N$ components constitute the sub-vector of measureable ion activities $\mathbf{a}^{(mes)}$, while subsequent $I - N$ components – the sub-vector of non-measureable ion activities $\mathbf{a}^{(nmes)}$. Let us also assume, that the number of sensors is equal to the number of measureable ions (i.e. $M = N$). Let us also denote with $\mathbf{v}$ a $N$-element vector with the following components:

$$v_i = 10^{z_i \frac{U_i - U_{0,i}}{S_i}} \quad i = 1, \cdots, M \tag{12}$$

$U_i, U_{0,i}, S_i$ denote read-out value, offset voltage and slope parameter of the $i$-th sensor, respectively. For $M = N$ the least squares optimization problem (11) becomes a set of non-linear equations that can be cast in the following form:

$$v_i = \sum_{j=1}^{I} K_{i,j} a_j^{z_i/z_j}, \quad i = 1, \ldots, N \tag{13}$$

To simplify presentation even further let us assume equal charges of all ions in the vector $\mathbf{a}$. Then the non-linear equations (13) become a set of linear equations:

$$\underbrace{\begin{bmatrix} \mathbf{K}^{(mes)} & \mathbf{K}^{(nmes)} \end{bmatrix}}_{\mathbf{K}} \cdot \underbrace{\begin{bmatrix} \mathbf{a}^{(mes)} \\ \mathbf{a}^{(nmes)} \end{bmatrix}}_{\mathbf{a}} = \mathbf{v} \tag{14}$$

where $\mathbf{K}^{(mes)}$ is the $N$ by $N$ sub-matrix of the matrix $\mathbf{K}$ of all selectivity coefficients, corresponding to the vector $\mathbf{a}^{(mes)}$ of measureable ion activities. $\mathbf{K}^{(nmes)}$ is the remaining part of the matrix $\mathbf{K}$, that corresponds to non-measureable ions.
The estimate obtained with the DF-PCM method, and denoted with vector $\mathbf{a}^{(mes,DF)}$, is obtained from (14) by assuming, that no non-measureable ions are present in the sample.

$$\mathbf{a}^{(mes,DF)} = \left[\mathbf{K}^{(mes)}\right]^{-1} \cdot \mathbf{v} \tag{15}$$

The vector $\Delta^{(DF)}$ of inaccuracies (systematic errors) for DF-PCM estimate $\mathbf{a}^{(mes,DF)}$ (and caused by presence of non-measureable ions) can thus be found from (14) and (15) as:

$$\Delta^{(DF)} = \mathbf{a}^{(mes,DF)} - \mathbf{a}^{(mes)} = \left[\mathbf{K}^{(mes)}\right]^{-1} \cdot \mathbf{K}^{(nmes)} \cdot \mathbf{a}^{(nmes)} \tag{16}$$

For the basic PCM method the estimate of measureable ion activities is expressed as:

$$\mathbf{a}^{(mes,PCM)} = \mathbf{v} \equiv \mathbf{K}^{(mes)} \cdot \mathbf{a}^{(mes)} + \mathbf{K}^{(nmes)} \cdot \mathbf{a}^{(nmes)} \tag{17}$$

Thus the error vector of this estimate can be expressed as follows:

$$\Delta^{(PCM)} = \mathbf{a}^{(mes,PCM)} = \mathbf{a}^{(mes)} = \underbrace{\Delta\mathbf{K} \cdot \mathbf{a}^{(mes)}}_{\Delta^{(PCM,1)}} + \mathbf{K}^{(nmes)} \cdot \mathbf{a}^{(nmes)} \tag{18}$$

where $\Delta\mathbf{K} \equiv \mathbf{K}^{(mes)} - \mathrm{diag}(\mathbf{K}^{(mes)}) = \mathbf{K}^{(mes)} - \mathbf{I}_N$ and $\mathbf{I}_N$ is the $N$ by $N$ diagonal matrix of ones. Let us note, that components of the PCM error vector are always non-negative, because all entries in selectivity matrices and ion activity vectors are non-negative. This is not the case for the DF-PCM, because the inverse to the selectivity matrix, i.e. $\left[\mathbf{K}^{(mes)}\right]^{-1}$, has negative off-diagonal elements; the sign of the error is thus dependent on actual values of the vector $\Delta^{(nmes)} \equiv \mathbf{K}^{(nmes)} \cdot \mathbf{a}^{(nmes)}$.

Comparing (16) and (18) one can consider the following conditions:

1. The number of sensors is equal to the number of ions ($M = I$).
2. Activities of non-measureable ions $\mathbf{a}^{(nmes)}$ are all zeros.
3. Sensors are ideally selective towards non-measureable ions (i.e. $\mathbf{K}^{(nmes)} = \mathbf{0}$).

Under each of the above conditions the DF-PCM estimate is exact, but the basic PCM estimate exhibits a non-negligible systematic error – denoted in (18) with $\Delta^{(PCM,1)}$. This inaccuracy goes to zero only when sensors are ideally selective (i.e. when $\mathbf{K}^{(mes)} = \mathbf{I}_N$ or equivalently $\Delta\mathbf{K} = \mathbf{0}_N$).

Insensitivity of DF-PCM to non-ideal sensor selectivity towards measureable ions, which was already shown and explored by the author in [3,11], favours DF-PCM over PCM – when actual measurement setup satisfy the above specified conditions. However, the winner is not that clear when sensors exhibit finite selectivity towards non-measureable ions. One can see in (16) and (18) that accuracy of both techniques is affected by the same term $\mathbf{K}^{(nmes)} \cdot \mathbf{a}^{(nmes)}$, but the corresponding error terms differ. The case study below gives more insight into the difference of inaccuracy.

**Case study**

$I = 3$ ions of unit charge number are assumed with activities in the range $10^{-2}$ to $10^{-5}$ mol/l; the first $M = 2$ ions are measureable by $N = 2$ sensors. Three matrices, containing sensor selectivity, are considered.

**Case A.** The first $\mathbf{K}$ matrix:

$$\mathbf{K}_A = \begin{bmatrix} 1.000 & 0.001 & 0.001 \\ 0.001 & 1.000 & 0.001 \end{bmatrix} \tag{19}$$

describes sensors of fair selectivity towards all ions. Accuracy of both PCM and DF-PCM is expected to be good.

**Case B.** The second $\mathbf{K}$ matrix:

$$\mathbf{K}_B = \begin{bmatrix} 1.000 & 0.100 & 0.001 \\ 0.001 & 1.000 & 0.001 \end{bmatrix} \tag{20}$$

represents much lower selectivity of the first sensor towards the second ion. DF-PCM is expected to perform better, improving on accuracy of the first ion estimate by taking advantage of better accuracy of the second ion estimate.

**Case C.** Description of the first ion in the third selectivity matrix:

$$\mathbf{K}_C = \begin{bmatrix} 1.000 & 0.100 & 0.000 \\ 0.000 & 1.000 & 0.010 \end{bmatrix} \tag{21}$$

shows ideal selectivity towards the third ion, and the same low selectivity towards the second ion. Second sensor is perfectly selective towards the first ion, but interference from the third ion can be expected. It is hard to bet on winner of accuracy comparison. Monte Carlo simulation with 1000 samples was set up to investigate accuracy of DF-PCM and PCM. Activities of the three ions were selected randomly. A sequence of 3000 random numbers, uniformly distributed in the interval $[-5; -2]$, was transformed (by $10^x$ function) to the interval $[10^{-2}; 10^{-5}]$. For each triple of the consecutive numbers

the vector **a** was formed, and then PCM and DF-PCM estimates and their inaccuracies were calculated.

To visualise accuracy of the two competitors the following component-wise ratios of (relative) inaccuracies were calculated for each sample:

$$\eta_1 = \left|\frac{\Delta_1^{(DF)}}{a_1}\right| \Big/ \left|\frac{\Delta_1^{(PCM)}}{a_1}\right| = \left|\frac{\Delta_1^{(DF)}}{\Delta_1^{(PCM)}}\right|, \quad \eta_2 = \left|\frac{\Delta_2^{(DF)}}{\Delta_2^{(PCM)}}\right| \tag{22}$$

Results of these calculations are shown in Fig. 3 - Fig. 5.

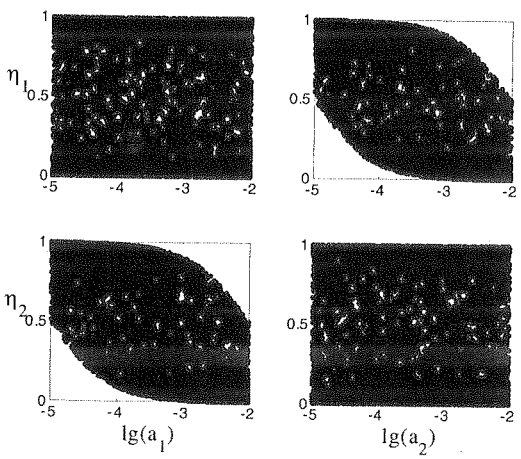


Fig. 3. Dependence of figures of merit ($\eta_1$ – the upper row, $\eta_2$ – the lower row of plots) on activities of the measureable ions for case A

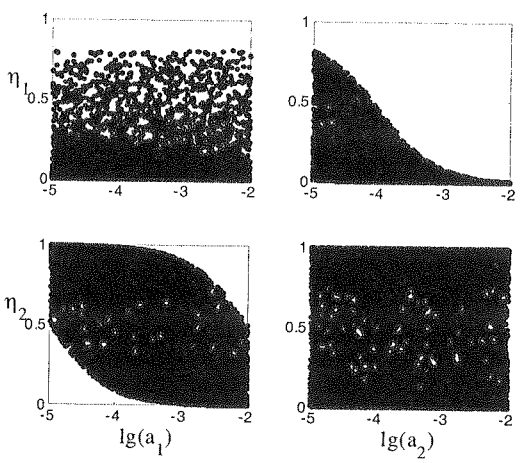


Fig. 4. Dependence of figures of merit ($\eta_1$ – the upper row, $\eta_2$ – the lower row of plots) on activities of the measureable ions for case B

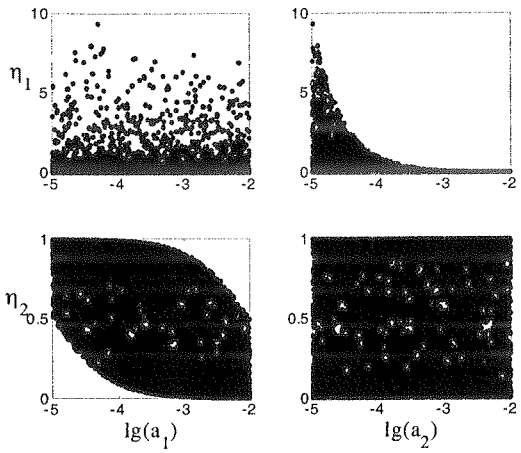


Fig. 5. Dependence of figures of merit ($\eta_1$ – the upper row, $\eta_2$ – the lower row of plots) on activities of the measureable ions for case C

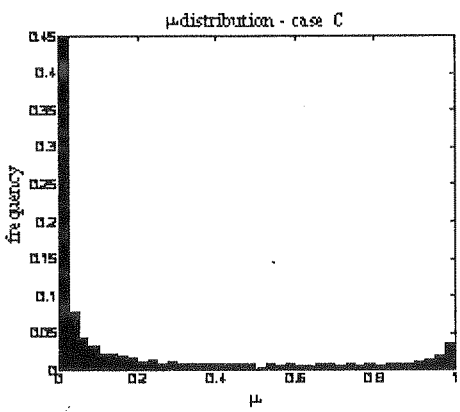


Fig. 6. Distribution of $\mu$ figure of merit for the selectivity matrix $\mathbf{K}_C$

For cases A and B the component-wise accuracy ratios belong to the interval [0; 1], i.e. accuracy of DF-PCM is not worse than PCM for all samples. Situation is different for case C, though (see Fig. 5). The value of $\eta_1$ can be significantly larger than 1, suggesting that PCM obtains better estimation accuracy of the first, while DF-PCM of the second, ion activity.

For the same samples another figure of merit was calculated – ratio of Chebyshev norm of relative inaccuracy for DF-PCM and PCM estimates:

$$\mu = \frac{\delta^{(DF)}}{\delta^{(PCM)}}, \text{where} \delta^{(DF)} = \max_{i=1,\ldots,N} \left| \frac{\Delta_i^{(DF)}}{a_i} \right|, \delta^{(PCM)} = \max_{i=1,\ldots,N} \left| \frac{\Delta_i^{(PCM)}}{a_i} \right| \tag{23}$$

One can see in Fig. 6, that value of $\mu$ is contained in the [0; 1] range. It means that for each of these samples, which expressed previously higher inaccuracy for some component of DF-PCM estimate vector, the other component was estimated much less accurately by PCM and that other component inaccuracy determined overall larger inaccuracy of PCM for that sample. Thus DF-PCM is a winner also in case C.

To give yet more insight into distribution of inaccuracy – another comparison was set up for the same Monte Carlo experiment. For water monitoring application it is typical to require 10% relative inaccuracy from ion measurement instruments. Thus this time estimates at all the 1000 samples points were checked for satisfying requested (10%) accuracy. Coordinates of the samples, which satisfy the requirement, are shown in Fig. 7-Fig. 9 with 'x' marks. It is seen in all the three cases, that DF-PCM provides larger area, named here "the acceptability region", which contains samples corresponding to ion estimates of sufficiently good accuracy (here: 10%). Again DF-PCM is shown to provide estimates with better accuracy than that for PCM estimates.

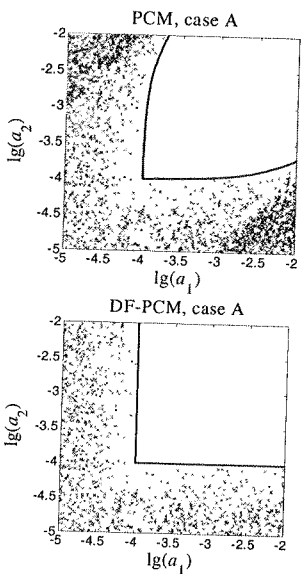


Fig. 7. Location of samples that do not satisfy 10% accuracy requirement for case A. Boundary of the acceptability region is shown with dashed lines

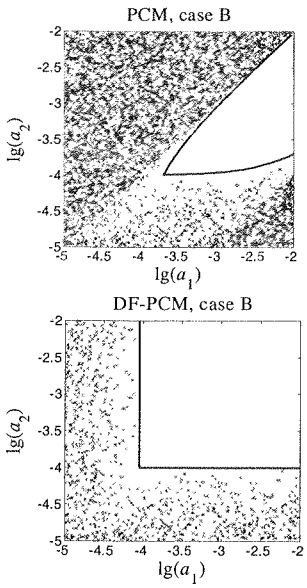


Fig. 8. Location of samples that do not satisfy 10% accuracy requirement for case B. Boundary of the acceptability region is shown with dashed lines

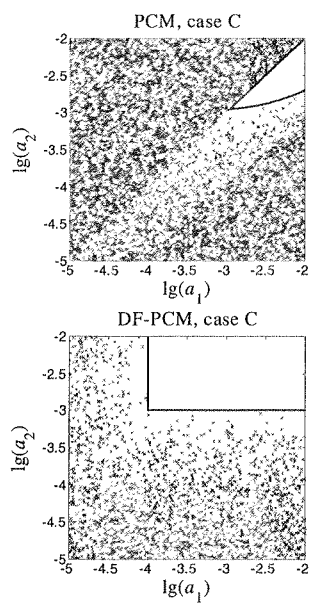


Fig. 9. Location of samples that do not satisfy 10% accuracy requirement for case C. Boundary of the acceptability region is shown with dashed lines

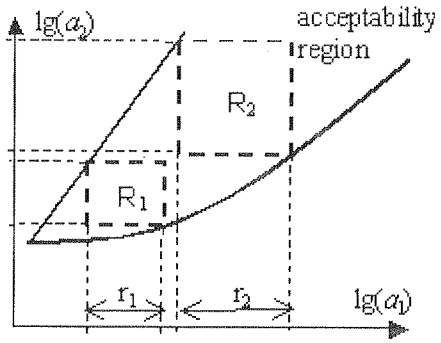


Fig. 10. Illustration of the measurement range definition problem for 2-sensor basic PCM procedure

### 2.4. INACCURACY OF SINGLE AND MULTI-SENSOR PCM TECHNIQUES

The last experiment enabled important comments on measurement ranges in multi-sensor chemical measurements. It is customary for a user of a measurement instrument, to expect from a manufacturer to specify a range of measureand values that can be found with assumed inaccuracy (be it 10% in our case). It is seen from our case study, that the lower end of such an interval can be specified for each component of DF-PCM estimate vector independently. For PCM this is not the case – measurement ranges for the first two ions are interdependent.

This situation can be described analytically as follows.

Let us denote the range of variation for each of ion activity as $[\underline{a}_i;\overline{a}_i]$, $i = 1,...,N$ (in our case study $\underline{a}_i = 10^{-5}$, $\overline{a}_i = 10^{-2}$, $N = 2$). Considering (16) we obtain:

$$\Delta^{(DF)} = \frac{a_3}{1 - K_{12}K_{21}} \begin{bmatrix} K_{13} - K_{12} \cdot K_{23} \\ K_{23} - K_{13} \cdot K_{21} \end{bmatrix} \tag{24}$$

$K_{i,j}$ denotes the element of the selectivity matrix (see (19)-(21)) which is at the cross-section of the $i$-th row and $j$-th column in the selectivity matrix $\mathbf{K}$. Assuming that $K_{12}K_{21} < 1$ in (24) – the requirement: $\mu \le \overline{\mu} = 10\%$ on relative accuracy of DF-PCM, expressed with (23), can be written as the following set of inequalities:

$$-a_1 \le \frac{a_3 \cdot (K_{13} - K_{12} \cdot K_{23})}{\overline{\mu} \cdot (1 - K_{12} \cdot K_{21})} \le a_1, \quad -a_2 \le \frac{a_3 \cdot (K_{23} - K_{13} \cdot K_{21})}{\overline{\mu} \cdot (1 - K_{12} \cdot K_{21})} \le a_2 ,$$
$$\text{for all } a_3 \in [\underline{a}_3;\overline{a}_3] \tag{25}$$

For the case C of our study we end up with the two inequalities, defining "the acceptability region":

$$a_1 \ge \frac{10^{-3}}{0.999} \cdot \frac{\overline{a}_3}{\overline{\mu}} \approx 10^{-4}, \quad a_2 \ge \frac{10^{-2}}{0.999} \cdot \frac{\overline{a}_3}{\overline{\mu}} \approx 10^{-3} \tag{26}$$

One can see agreement of inequalities (26) and the acceptability region obtained by simulation (see Fig. 9). The inequalities (26) determine the lower end of the measurement range for DF-PCM – independently for each measureable ion. The upper range is determined in practice by increase of sensor model ((1),(5)) inaccuracy for higher level of the main ion concentration, that is caused by interference from ions of opposite charge sign (counter-ions). For users interested in ion concentration (and not activity) – the upper side of the measurement range is related to possible change (increase) of the ionic strength due to large concentration increase of any (or both) ions.

We can perform similar derivation for the basic PCM technique, considering inaccuracy expression (18). Instead of inequalities (25) we get the following ones:

$$|K_{12} \cdot a_2 + K_{13} \cdot a_3| \leq \bar{\mu} \cdot a_1, \quad |K_{21} \cdot a_1 + K_{23} \cdot a_3| \leq \bar{\mu} \cdot a_2 \ , \text{forall} a_3 \in [\underline{a}_3; \bar{a}_3] \quad (27)$$

For the case C the "acceptability region" is defined by:

$$a_2 \leq \frac{\bar{\mu}}{0.1} a_1 \equiv a_1, \ a_2 \geq \frac{0.01}{\bar{\mu}} a_1 + \frac{0.01}{\bar{\mu}} \bar{a}_3 \equiv 0.1 \cdot a_1 + 10^{-3} \quad (28)$$

Again, agreement with the simulation can be noticed (see Fig. 9).

Let us note, that for PCM accuracy constraints restrict measureable ions jointly (and not one at a time as is the case for DF-PCM). This creates a problem, when determining measurement range – as illustrated in Fig. 10. When we select rectangle $R_1$ to represent pairs $(a_1, a_2)$ of ion activities, for which estimation inaccuracy stays within presumed limit $(\bar{\mu})$ – then measurement ranges are just projections of $R_1$ onto both axes. For the first ion we thus have measurement range $r_1$, as shown in Fig. 10. But instead of $R_1$ we might as well use $R_2$ – ending up with completely different measurement ranges (see $r_2$ in Fig. 10). Thus it was demonstrated, that for the basic PCM approach it is rational not to represent measurement ranges in a traditional way – with fixed width intervals, independent for each ion. Instead, formulae should be provided, that express relationships among endpoints of intervals for each ion. This is in fact equivalent to symbolic representation of the border to the measurement acceptability region (for given maximum inaccuracy level).

## 3. CONCLUSIONS

The paper presented comparison of two multi-sensor measurement techniques, called basic PCM and DF-PCM. The latter one was shown to provide superior systematic inaccuracy and clearer measurement range specifications. The problem of entangled measurement ranges was presented for the PCM approach, and a rational solution was shown.

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